SERVICE MANUAL

(MODEL: SD840 SERIES)

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1

SYSTEM SPECIFICATION

1.1 INTRODUCTION

This system is a powerful computer that offers the high performance and power of 33MHz 80386 microprocessor designed into a compatible IBM AT architecture. A socket is prepared for the numeric coprocessor Intel 80387 or Weitek 3167 for the specific applications which requier fast real time processing capability such as CAD system or engineering workstation. With its 8 I/O slots, it provides an outstanding performance and features for your specific applications. The performance is increased by three to four times over 8MHz 80286-based personal computers. The system mother board is approximately 30.5 by 33 centimeters (12.6 by 13 inches) and the board is a 8-layer PCB (Printed circuit Board) to maximize the system reliability while reducing the EMI (Electro-Magnetic Interfaces).

The system mother board contains the ATLAS Chip Set (it is also called as GCK131 Chip Set: GC131, GC132, and GC133), of three highly integrated HCMOS microchips, which supports an 80386 microprocessor-based computer system in AT-compatible mode at speeds up to 33MHz.

This high performance three chip set allows the implementation of a powerful computer system with just these components: an 80386 microprocessor, a keyboard controller, a real time clock, six bipolar devices and up to 24M of memory.

Note: ATLAS (HT131, HT132, and HT133), the name of chip set, is mingled with GCK131 (GC131, GC132, and GC133) in this book. HT131 Peripheral Controller chip has the same function with GC131. HT132 CPU/Memory Controller also has the same function with GC132, and HT133 Bus Bridge Interface does with GC133.

1.2 SYSTEM OVERVIEW

The main unit enclosed with metal housing to comply with FCC regulations and safety standards has the following features;

1. System motherboard running at 33MHz (with 4MB DRAM)
2. A 5.25" (1.2MB formatted) and a 3.5" (1.44MB formatted) floppy disk drives
3. Graphics adapter
4. Power supply (275 watts)
5. A keylock switch to prevent your computer from any unauthorized access
6. Two cooling fans for system reliability; installed in the power supply and the front of the chassis
7. Fixed disk drive: option

A 101-key keyboard comes with the computer and all IBM-AT compatible peripherals such as monitor, printer, plotter, and modem and allowed to be attached to the computer for your best applications.

1.3 OVERALL SPECIFICATION

1.3.1 System Board

CPU
INTEL 80386-33MHz
Full 32-bit data path
INTEL iAPX 88/86/286/386 instruction set
Real and Virtual address mode

ATLAS Chip Set
HT131 (or GC131) Peripheral Controller
HT132 (or GC132) CPU/Memory Controller
HT133 (or GC133) Bus Bridge Interface

Memory
Onboard 4MB standard (Expandable to 24MB)

Expansion Slots
8 I/O slots: 2 8-bit slots
6 16-bit slots

Real Time Clock
DS1287 real time clock CMOS chip with integral lithium battery

Floppy Disk Controller
8473 Floppy disk controller supporting 3.5″ and 5.25″ drives

I/O Ports
One parallel, two serial ports and one PS/2 mouse port are embedded

Numeric Coprocessor Socket
A socket is provided for INTEL 80387 or WEITEK 3167 coprocessor

1.3.2 Floppy Disk Drive

5.25″ FDD
half-height
1.2MB formatted
96 TPI (Tracks/Inch)
3ms track-to-track access time
500 kbits/sec transfer rate

3.5″ FDD
1″(H)×4″(W)×5.9″(D)
1.44MB/720KB formatted
135 TPI (Tracks/Inch)
6ms track-to-track access time
500 kbit/sec transfer rate (1.44MB mode)
250 kbit/sec transfer rate (720KB mode)

1.3.3 Graphics Adapter

Monochrome Graphics Adapter
supports monochrome graphics mode
32KB of video memory
uses industry standard 9-pin 'D' connector

Text mode:
720×340 resolution
7×9 cell characters in a 9×14 cell character block
supports PC attributes – underline, reverse, and highlight

Graphics format:
720×340 dot-addressable pixels

Enhanced Graphics Adapter
supports enhanced color graphics mode
256KB of video memory
uses industry standard 9-pin 'D' connector

Text mode:
80 char×25 lines resolution
8×14 character box

Graphics format:
640×350 dot-addressable pixels
16 color graphics from a pallet of 64 colors

Video Graphics Array
All video modes available in the IBM Monochrome Display Adapter, IBM Color Graphics Adapter, and IBM Enhanced Graphics Adapter are supported, regardless of which analog display is connected.

The new modes available are;
640×480 graphics in both 2 and 16 colors
720×400 alphanumeric in both 16-color and monochrome
360×400 16-color alphanumeric
320×200 graphics with 256 colors

1.3.4 I/O Ports

Two serial and one parallel I/O ports are built-in on the mother board, which can be disabled if necessary.

1.3.5 PS/2 Mouse Port

A PS/2 mouse port is provided on the system mother board.

1.3.6 Software

MS-DOS version 4.01 and GW-BISIC comes with the system. Almost all of the softwares written for the IBM personal computers run on your computer with full compatibility but faster.

2

BOARD OVERVIEW

2.1 INTRODUCTION

This chapter provides an overview of the system board. Included in this chapter is a list of features, a block diagram of the board, and a description of the feature set.

2.2 OVERVIEW

The system board contains the fallowing components:

- 33MHz 386 central processing unit (CPU)
- A numeric coprocessor socket (Intel 80387 or Weitek 3167)
- 64K cache memory (Expandable up to 128K)
- A 38202 cache controller
- Standard 4MB of random access memory (DRAM) (Expandable up to 24M)
- 256K read only memory (ROM)
- GCK131 Chip set (made by LSI Logic)
- DS1287 real-time clock/calendar with integral lithium battery
- 16C452 I/O port controller and ports (2 serial and 1 parallel)
- 8742 Keyboard/Mouse controller and connectors
- IDE interface logic and connector
- 8473 Floppy disk drive controller and connector
- Eight I/O expansion slots (two 8-bit, six 16-bit)

- ROM based setup program, BIOS, and power-on self test
- Reset interface
- Speaker interface
- Keylock interface

Figure 2-1 illustrates the component layout of the system board. Figure 2-2 shows a functional block diagram of the system board.

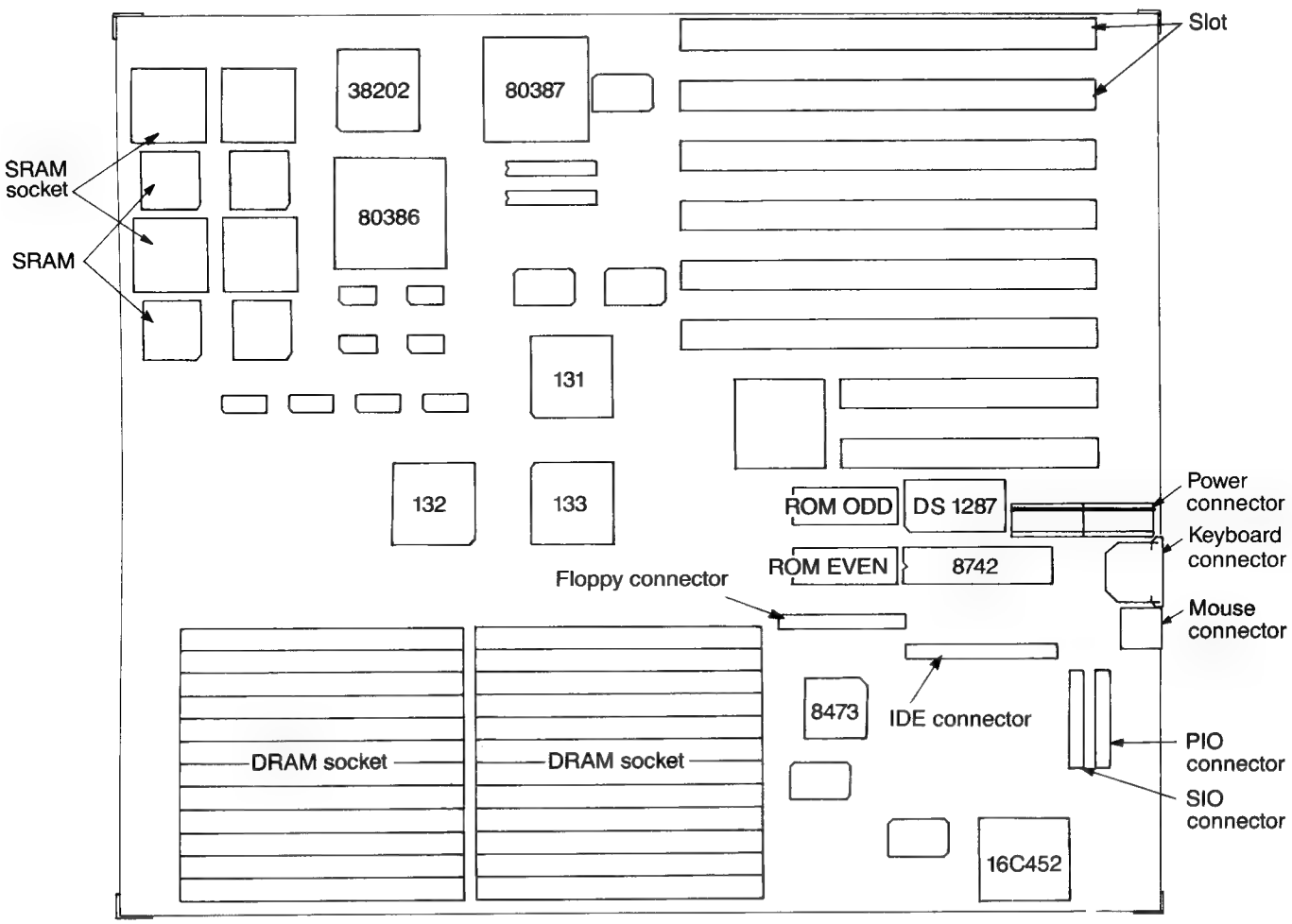


Figure 2-1. System Board Component Layout

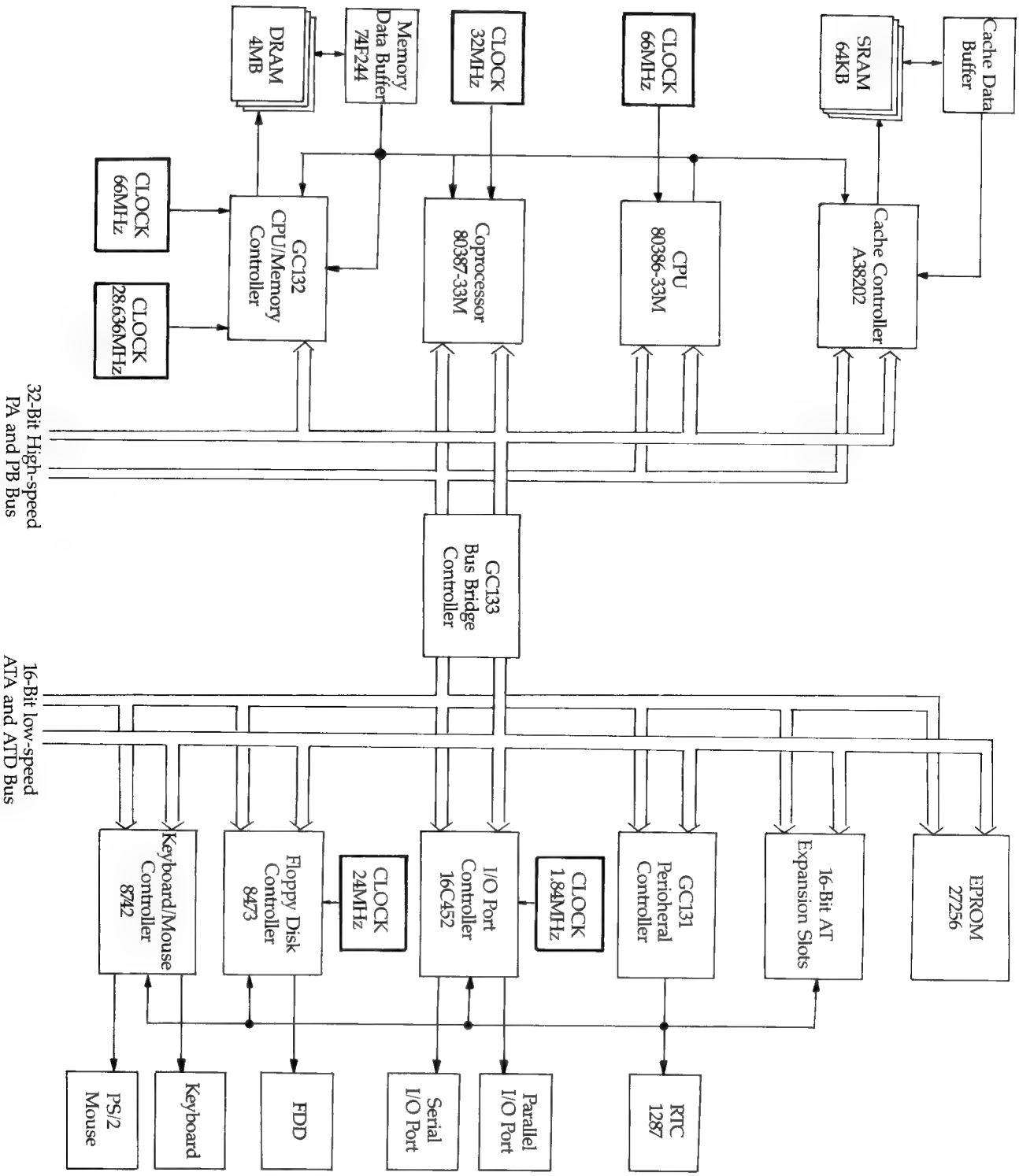


Figure 2-2. System Board Functional Diagram

2.3 FEATURE SET DESCRIPTION

This section gives a detailed description of the features listed earlier.

2.3.1 Central Processing Unit (CPU)

The CPU incorporates multitasking support, memory management, address translation caches, and a high speed 32-bit bus interface. The CPU must runs at a clock speed of 33.3MHz resulting in a system speed of 30ns per clock cycle. For applications requiring slower operation (such as installing some copy-protected software) the system provides a deturbo (slow) mode reduces the effective system operating speed to 8MHz.

2.3.2 Memory

The system board contains three types of memory: ROM, cache memory, fag memory, and DRAM.

- The system board contains 256K of ROM containing the BIOS, power-on self test (POST) and setup program.
- The 64K direct-mapped cache memory consists of eight static random access memory (SRAM) chips. The cache provides zero wait-state read performance and one wait-state write performance during CPU accesses. The cache tag memory consists of three SRAM chips and supplies 12-bit tag data for address comparison.
- The system board contains 4M (expandable 24M) of DRAM.

2.3.3 ISA Bus

The system is compatible with the ISA bus. I/O expansion boards communicate with the system via ISA bus.

2.3.4 GCK131 Chip Set

GCK131 chip set consists of three chips: GC131 Peripheral controller, GC132 CPU/Memory controller, and GC133 Bus bridge interface.

GC131 Peripheral Controller

This single chip effectively replaces two 8259 programmable interrupt controllers (PICs), two 8237 direct memory access (DMA) controllers, an integrated circuit containing three general purpose programmable interval timers (PITs), an LS612, and other devices. The chip interfaces with an 8042 keyboard controller, real time clock, parallel ports, serial ports, speaker and the EEPROM used for power up configuration.

GC132 CPU/Memory Controller

This powerful chip decodes the processor address and control lines and generates RAS, CAS, and chip select signals required for memory management. Both static and dynamic memories can be used. The GC132 controller features both paged and interleaved memory access techniques that improve overall system throughput.

GC133 Bus Bridge Interface

This chip links AT address and data buses, the processor address and data buses and the memory bus.

2.3.5 DS1287 Real-time Clock (RTC)

The RTC provides 50 bytes of CMOS RAM and a battery backup power source for keeping system clock/calendar and system configuration parameters in non-volatile memory. This protects the contents of both the RAM and the clock during system power-up and power-down.

2.3.6 Input/Output Expansion Slots

The system has 8 I/O expansion slots:

- Two slots (J7, J8) accept 8-bit expansion boards only.
- Six slots (J1, J2, J3, J4, J5 and J6) accept 16-bit or 8-bit expansion boards.

2.3.7 Input/Output Ports

The system provides a parallel printer port configured as either LTP1 or LTP2 and serial communication ports configured as COM1 and COM2. Both serial ports are available on connector P20 and one parallel port is available on P22.

2.3.8 8742 Keyboard and PS/2 Mouse Controller

The keyboard connects to the system board through a bidirectional synchronous serial port. The bidirectional serial interface converts signals and sands the data to and from 101-key keyboard. A mouse can be connected via a mini-DIN (PS-2 style) connector on the system board.

2.3.9 IDE Interface Logic and Connector

The system mother board contains IDE (Intelligent Drive Electronic) logic and support circuitry and connector designated as P18.

2.3.10 8473 Floppy Disk Controller and Connector

The system mother board contains DP8473 floppy disk controller unit and connector designated as P15.

2.3.11 Special Board Interfaces

The system board incorporates four special interfaces: the keylock interface, the speaker interface, the reset interface, and the diagnostic LED interface.

2.3.12 Firmware

The system board firmware consists of a power-on self test (POST), a setup program, and Phoenix Technologies' basic input/output system (BIOS).

POST runs automatically and checks the CPU, keyboard, display, and system memory each time the system is turned on a rebooted.

The setup program is contained in the ROM BIOS on the system board and is used to store configuration information. The information can be changed at any time by running setup program. The type of configuration information maintained by the setup program is as follows:

- Date and time
- Number and capacity of floppy disk drives
- Amount of base and type of fixed disk drives
- Availability and type of primary monitor controller

- Keyboard present
- Numeric coprocessor present
- Shadow or do not shadow system BIOS and video BIOS
- Enable or disable cache memory, speaker and preboot setup

Onboard ROM consists of two 27256 EPROMs containing 64K of memory. The EPROMs contain the ROM code for the BIOS. Functions of the BIOS are as follows:

- System initialization
- Power-on diagnostics
- System configuration
- Disk bootstrap loading
- Character bit patterns of the ASCII character set
- Storage of frequently needed input and output routines

If enabled in setup, the BIOS initializes the DRAM-shadowed BIOS option for increased system performance.

3

CENTRAL PROCESSING CORE

3.1 INTRODUCTION

This chapter describes the central processing core of the system board. The 386 CPU, the 387 numeric coprocessor, cache memory, cache tag memory, and the data and control buffers are discussed. For more information on these components, refer to the Intel Microprocessor and Peripheral Handbook.

3.2 OVERVIEW

The central processing core contains the following components:

- A 386 32-bit CPU
- A 387 numeric coprocessor
- Cache memory
- Cache tag memory
- Data and control buffers

3.3 CPU

The CPU is 386 micro processor operationg at 33MHz with the speed of 30.3nS per clock cycle. The CPU has seperate 32-bit data and address paths, plus on-chip memory management and protection. The CPU supports multiuser and multitasking systems, memory management, virtual memory, and task or memory isolation. Refer to the rear of this manual for a list of Intel reference manuals that provide detailed information on the 386 microprocessor.

3.3.1 Real Mode Architecture

The CPU defaults to real mode upon reset. Real mode is compatible with 8086/8088 and 80286 CPUs at the object code level and has the same capability and limitations. In real mode, addressable physical memory is limited to 1M via segment registers, with 64K limitation on segment size. Real mode does not provide memory protection features.

Real mode address are formed, as in the 8086, by combining the base address from a segment register with the offset value procided by the instruction. The CPU shifts the 16-bit base address value in the segment register left four bits, and adds the 16-bit offset value forming 20-bit real address.

3.3.2 Protected Mode Architecture

Protected mode significantly increases the linear address space (to 4 gigabytes) and enables the running of virtual memory programs of almost unlimited size (64 terabytes). In this mode, the integrated memory management and protection mechanism tronslates virtual addresses to physical addresses. It also isolates the operating system and enforces protection rules necessary for remaining task integratin a multitasking environment. This is useful in a multitasking and multiuser environment where resources are shared.

Protected mode provides memory pasing, I/O protection, virtual 8086 mode, and a full 32-bit extended instruction set. Protected mode provides source code compatibility with the 8086/8088 and 80286 allowing direct execution of 16-bit applications at higher speeds.

3.3.3 Virtual-8086 Mode

The virtual 8086 mode is an extention of the protected mode. Under this mode, the CPU provides compatibility with applications developed for the 8086/8088 while simultaneously peoviding a full 32-bit, large linear address programming environment in its protected mode. Virtual memory allows programs to overcome the limitation of physical memory.

The system divides virtual memory into amny different segments. These segments are mapped into physical memory during virtual memory execution. The memory management system transfers code and data between physical memory and disk.

3.3.4 CPU Signals

The following text defines the signal functions of the CPU. A signal name followed by an "I" in parentheses indicates an input signal. A signal name followed by an "0" in parentheses indicates an output signal. A signal name followed by "I/O" in parentheses indicates an input/output signal. For more detailed information on the CPU signal functions, refer to the Intel Microprocessor and Peripheral Handbook.

CLK2 (I)

CLK2 is the clock input pin, CLK2 provides the fundamental timing for the 386, and is driven by a 66MHz crystal. CLK2 is divided by two internally to generate the internal processor clock used for instruction execution.

D31:0 (I/O)

D31:0 are the data bus signals. These tri-state bidirectional signals provide the general purpose data path between the 386 and other devices.

A31:2 (O)

A31:2 are the address bus sugnals. These tri-state outputs provide physical memory addresses or I/O port addresses for the system.

BE3:0* (O)

BE3:0 are the byte enable signals. These signals directly indicate which bytes of the 32-bit data bus are involved with the current teansfer.

ADS* (O)

ADS is the address status signal. This tri-state output indicates that a valid bus cycle definition, and an address (W/R*, D/C*, M/IO*, and BE3:0*, A31:2) is being driven at the 386 pins. ADS* is asserted during T1 and T2 bus states.

M/IO* (O)

M/IO* is the memory or I/O select signal. This tri-state signal distinguishes between memory and I/O cycles.

D/C* (O)

D/C* is the data or control select signal. This tri-state signal distinguishes between data and control cycles.

W/R* (O)

W/R* is the write or read select signal. This tri-state signal distinguishes between write and read cycles.

LOCK* (O)

LOCK* is the locked bus selection signal. This tri-state output distinguishes between locked and unlocked bus cycles.

BS16* (I)

BS16* is the bus size signal. This signal allows the 386 to directly connect to 32-bit and 16-bit data buses. Asserting this input constrains the current bus cycle to use only the lower half (D15:0) of the data bus, corresponding to BE0* and/or BE1*. Asserting BS16* has no additional effect if only BE0* are/or BE1* are asserted in the current cycle. However, during bus cycles asserting BE2* or BE3*, asserting BS16* will automatically cause the 386 to make adjustment w=s for correct transfer of the upper bytes using only physical data signals D15:0. If the operand spans both halves of the data bus and BS16* is asserted, the 386 will automatically perform another 16-bit bus cycle.

READY* (I)

READY* is the transfer acknowledge signal. This input indicates the current bus cycle is complete, and the active bytes indicated by BE3:0* and BS16* are accepted or provided. When READY* is sample asserted during a read cycle or interrupt acknowledge cycle, the 386 latches the input data and terminates the cycle. When READY* is sample asserted during a write cycle, the prodessor terminates the bus cycle.

HOLD (I)

HOLD is the bus hold request signal. This input indicates some device other than the 386 requires bus mastership. The device must keep HOLD asserted as long as it is a bus master. HOLD is level sensitive and is a synchronous input.

HLDA (O)

HLDA is the bus acknowledge signal. This output indicates the 386 has relinquished control of its local bus in response to HOLD being asserted, and is in the bus hold acknowledge state. In the bus hold acknowledge state, HOLD is the only signal bring driven by the 386. The other output or bidirectional signals are in a high-impedance state allowing the requesting bus master to control them.

INTR (I)

INTR is the maskable interrupt request signal. This input indicates a request for interrupt service, which can be masked by the 386 flag register IF but. When the 386 responds to the INTR input, it performs two interrupt acknowledge bus cycles, and at the end of the second, latches an 8-bit interrupt vector on D7:0 to identify the source of the interrupt. The CPU samples the INTR line at the beginning of each processing cycle. INTR must be active at least two processing cycles before the current instruction ends or it will be serviced during the next cycle. INTR is level sensitive and is asynchronous to the CLK2 signal.

NMI (I)

NMI is nonmaskable interrupt request signal. This input indicates a request for interrupt service that cannot be masked by software. NMI has priority over all other interrupts. NMI is rising edge sensitive and is asynchronous to the CLK2 signal.

PEREQ (I)

PEREQ is the coprocessor request signal. This signal indicates a coprocessor request for a data operand to be transferred to/from memory by the 386. In response, the 386 tranfers information between the coprocessor and memory. Because the 386 has internally stored the coprocessor opcode being executed, it performs the requested data transfer with the correct direction and memory address. PEREQ is level sensitive and is asynchronous to the CLK2 signal.

BUSY* (I)

BUSY* is the coprocessor busy signal. This input signal indicates the coprocessor is executing an instruction, and is not able to accept another. When the 386 encounters any coprocessor instruction which operates on the numeric stack (for example load, pop, or arithmetic operation), or the WAIT instruction, this input is automatically sampled until it is seen negated. This sampling of the BUSY* input prevents overrunning the execution of a previous coprocessor instruction. The CPU program execution stops as long as the BUSY* signal remains active. BUSY* is level sensitive and is asynchronous to the CLK2 signal.

ERROR* (I)

ERROR* is the coprocessor error signal. This input signal indicates the previous coprocessor instruction generated a coprocessor error of a type not masked by the coprocessor's control register. This input is automatically sampled by the 386 when a coprocessor instruction is encountered, and if asserted, the 386 generated exception 16 to access the error-handling software. ERROR* is level sensitive and as asynchronous to the CLK2 signal.

RESET (I)

RESET is the reset signal for the system. This input signal suspends any operation in progress and places the 386 in a known reset state. The 386 is reset by asserting RESET for 15 or more CLK2 periods (80 or more CLK2 periods before requesting self test). When RESET os asserted, all other pins are ignored. RESET is level sensitive and must be synchronous to the CLK2 signal.

3.3.5 Basic CPU Bus Operations

The bus control unit manages all bus operations. It generates the address, data, and command signals for external memory and I/O operations. The bus control unit also transfers instructions to the instruction pre-fetch unit. Instructions are stored in a 16-byte queue waiting for decoding and execution. The execution unit does not need to wait for the completion of a bus cycle before accepting a new instruction. This results in faster execution of instructions.

The instruction pre-decode unit receives and decodes the instructions from the prefetch queue. It places them in the decoded instruction queue for use by the execution unit.

The execution unit executes the basic processing functions. It accepts the decoded instructions from the instruction pre-decode unit and executes them. It used the bus unit to fetch and store operands during the execution of instructions.

The address paging unit and segmentation unit provide memory management and protection services for the CPU. These units also translate logical addresses into physical address for use the various memory translation and protection checks for each bus cycle (see Figure 3-1).

The CPU uses a 66.67MHz clock to control bus timing. The CPU divided this clock by two producing the internal processing clock and determining the bus cycle speed.

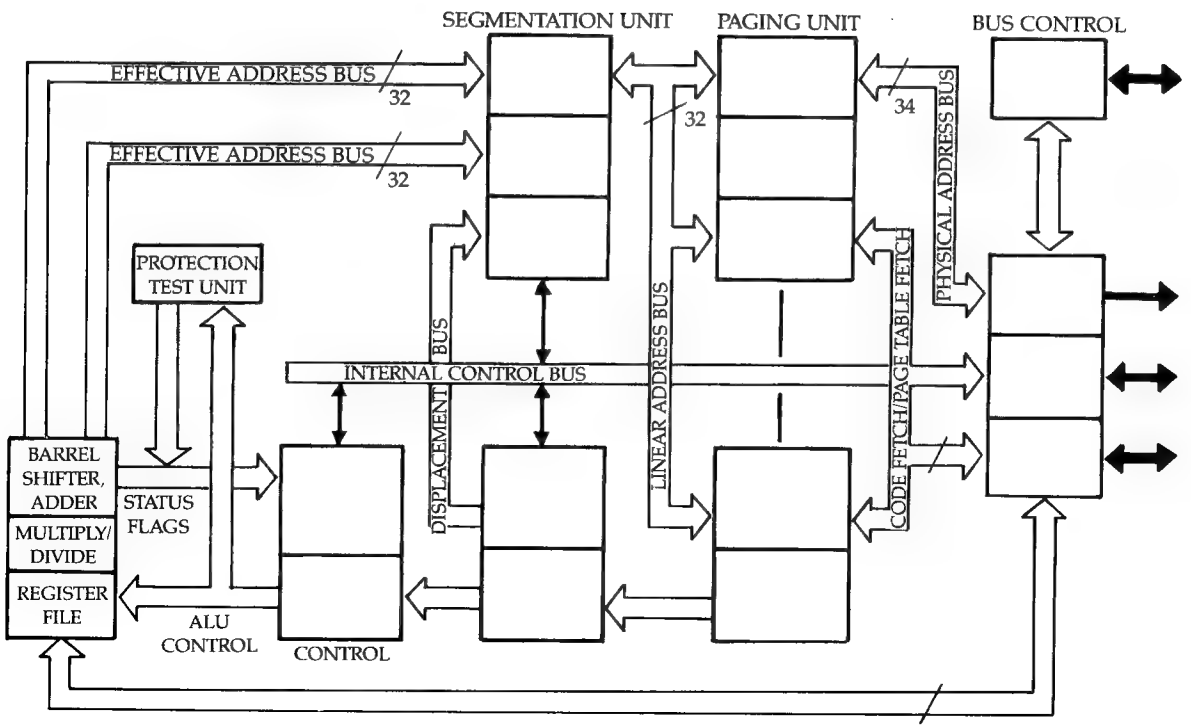


Figure 3-1. CPU Block Diagram

3.4 NUMERIC COPROCESSOR

A 121-pin extended numeric coprocessor (ENP) socket installe on the system board accommodates either an Intel 80387 or Weitek 3167 numeric coprocessor. Both use the same clock generator as the CPU and fully support signal, double, and extended precision operations.

The system board executes high-speed methematical calculations, logarithmic functions, and trigonometric operations using the numeric coprocessors. The numeric coprocessors operate syncronously with the CPU.

Both numeric coprocessors provide the CPU with additional data types, register, instructions, and interrupts specifically designed to support high speed numeric coprocessing. The register in the numeric coprocessor hold constants and temporary results generated during calculations. These registers reduce memory access time and increase speed and bus availability. Numeric coprocessor register space can be used as a stack or fixed register set.

3.4.1 387 Data Types

The 387 numeric coprocessor fully implements ANSI/IEEE 754 standard for binary floating-point arithmetic. It works with seven data tupes: word integer, short integer, long integer, packed decimal, single real, double real, and extended real (refer to Table 3-1).

The 387 directly extends the CPU instruction set. Extending the instruction set includes trigonometric, logarithmic, exponential, and arithmetic instructions for all data types.

Table 3-1. 387 Numeric Coprocessor Data Types

Data Type	Bits	Digits	Approximate Range
Word integer	16	4	$-32{,}768 \leq x \leq +32{,}767$
Short integer	32	9	$-2\times10^{9} \leq x \leq +2\times10^{9}$
Long integer	64	18	$-9\times10^{18} \leq x \leq +9\times10^{18}$
Packed decimal	80	18	$-9\ldots99 \leq x \leq +9\ldots99$ (18 digits)
Single real	32	6:7	$1.18\times10^{38} \leq x \leq 3.40\times10^{38}$
Double real	64	15:16	$2.23\times10^{-308} \leq x \leq 1.80\times10^{308}$
Extended realt	80	19	$3.30\times10^{-4932} \leq x \leq 1.21\times10^{4932}$

Equivalent to double extended format of IEEE STD 754.

3.4.2 387 Programming Interface

The 387 functions as an I/O device through the I/O ports. It uses hex addresses 8000FC for sending upcodes and operands and also receiving and storing results. The CPU outputs address 8000F8 when writing a command or reading status and outputs address 8000FC when writing or reading data.

The CPU has three input signals for controlling data transfer to and from the 387 numeric coprocessor: BUSY*, PEREQ (387 request), and ERROR*. These input signals connect to the corresponding 387 pins.

The BUSY* signal informs the CPU that the 387 is executing an instruction and cannot accept another. The CPU WAIT instruction informs the CPU to wait until the 387 finishes execution. The PEREQ signal indicates the 387 needs to transfer data. Because the 387 is never a bus owner all input and output data transfers are done by the CPU. PEREQ always goes inactive before BUSY* goes inactive.

The 387 asserts an ERROR* signal after an instruction results in an error not masked by the 387 control register. If an error occurs, ERROR* goes active. As a result, the CPU receives an interrupt. If a higher priority does not exist, the CPU services the interrupt.

The 387 detects six different classes of exception conditions that may occur during instruction execution. If the proper execution mask is not set by the control register, the 387 asserts an ERROR* signal. The signal generates a hardware interrupt (BUSY*) holding the 387 in a busy state until cleared by the execution of an FNINIT instruction.

The numeric exception conditions recognized by the 387 are as follows:

1. Invalid operations (stack fault or IEEE standard invalid operation)
2. Divide-by-zero
3. Denormalized operand
4. Numeric powerflow
5. Numeric underflow
6. Inexact result (precision)

POST code in the system ROM enables the hardware interrupt. It also sets the hardware interrupt vector pointing to a routine in ROM. This routine clears the latch on the BUSY* signal and generates an IRQ13 interrupt.

While the CPU executes numeric programs in either real or protected mode, interrupts report exception conditions. Refer to the 80387 Programmers Reference Manual (Intel order number 231917-001) for detailed descriptions of 387 interrupts and exceptions.

All communication between the CPU and the 387 is transparent to applications software. The 387 operates whether the CPU executes instructions in real-address mode, protected mode, of virtual 8086 mode. The CPU handles all memory accesses. The 387 operates on instructions and values passed to it by the CPU and is not aware of the processing mode of the CPU.

For complete information on programming the 387, refer to the 80387 Programmer's Reference Manual (Intel order number 231917-001).

3.4.3 Weitek 3167 System-Level Considerations

The Weitek 3167 is a memory-mapped numeric coprocessor communicating with the CPU over the processor address bus. Instructions are defined by the 14 least-significant address bits (A15:2) and three of the four byte-enables (BE2:0).

Addresses A31-A25 and M/IO select the 3167. Address bits A31 and A29 determine the 3167 operation requests.

The 3167 decodes memory addresses C0000000 through C1FFFFFF. Although addresses C0000000 to C000FFFF are normally unused, it is important that other components in the system do not conflict with the address space used by the 3167. Reading and writing to this address apace causes the 3167 to drive the data bus and execute instructions respectively.

3.5 CACHE MEMORY

The cache memory and cache tag memory implement a 2-way set associative 64K write-through cache for the CPU.

The cache is located beside the CPU and holds information contained in the system memory for fast CPU access. The cache contains 64K of memory organized into 16K words of 32 bits per word. It also uses a 2-way set associative design with posted write through to main memory on all write cycles. The CPU accesses cache memory information on reads at full speed with no wait states. The CPU accesses write hits with one wait state.

Four 8K×16 30ns SRAMs comprise the memory portion of the cache. The SRAMs make up the 32-bit word for the bus and are addressed by the least-significant 14-bits of the address bus.

3.6 DATA AND CONTROL BUFFERS

Bidirectional buffers transfer control, data, and address signals between the CPU bus and the ISA bus. Four buffers transfer CPU data, D(31:0), and four buffers transfer CPU addresses, A(27:02).

4

ISA BUS INTERFACE

4.1 INTRODUCTION

This chapter provides an overview of the ISA bus interface as implemented on the system board.

4.2 BUS AGENTS

The ISA bus allows several different bus agents. A bus agent is a physical unit which has an interface directly to the ISA bus. A memory expansion board, a LAN controller, and a modem are all examples of bus agents. The two basic types of bus agents are Requesting Agents and Replying Agents.

4.2.1 Requesting Agents

Requesting agents initiate an ISA bus cycle. Requesting agents can be either a Primary Requesting Agent (PRA) or an SRA.

The PRA has immediate access to the ISA bus when control has been granted to an SRA. The only PRA allowed is the system board.

The SRA is an optional Requesting Agent that normally does not have immediate control of the ISA bus. Control of the bus is requested from the PRA. Multiplex. SRAs are allowed. An SRA must have a 16 bit bus interface. No 8-bit SRA's are allowed on the ISA bus.

4.2.2 Replying Agents

A replying agent responds to ISA bus cycles when initiated by a requesting agent. A replying agent cannot initiate ISA bus cycles.

4.2.3 Configuring Bus Agents

The ISA bus services 11 agents via 8-bit and 16-bit portions of the bus. The number of each agent type that is suported is as follows:

Agent	1-11 (PRA + 10)
Requesting agent	1-10 (PRA +9)
PRA	1 (PRA)
SRA	0-9
Replying agent	0-10

4.2.4 Agent Function Model

Table 4-1 describes the types of ISA bus cycles in which ISA bus agents may participate.

Table 4-1. ISA Bus Cycles

Type of Agent	Agent's Action
Primary Requesting agent	Initiates: Memory access I/O access DMA access Global refresh Responds to: Interrupt request DMA request Bus arbitration request
Secondary Requesting agent	Initiates: Memory access I/O access Responds to: Global refresh Gains Bus Ownership by: DMA request Assuming bus ownership on DMA grant Assuming responsibility for refresh initiation
Replying agent	Responds to: Memory access I/O access DMA access Global refresh Seeks PRA serice through: Interrupt request DMA request

4.3 GENERAL ISA BUS ATTRIBUTES

The ISA bus has several specific attributes as follows:

- The memory address space is 24 bits long and the data path is 16 bits wide, providing a 16M memory address space with 8 and 16-bit data transfers.
- The I/O address space is 16 bits long and the data path is 16 bits wide, providing a 64K I/O address space with 8-bit and 16-bit data transfers.
- Interrupt lines suport signalling between agents on the bus and the PRA.
- The DMA capability allows 8-bit or 16-bit data transfers between memory and I/O agents without direct intervention of the CPU on the PRA.
- The PRA refershes all agents with refresh cycles. The PRA initiates refresh cycles at the request of an SRA that is in control of the bus in order to maintain integrity of the data in system DRAM.
- Multiple agent support is provided. The ISA bus Suports up to five agents, including one PRA and up to a total of four SRAs and replying agents. A PRA (the 303 board itself) is required in all implementations. SRAs and replying agents are strictly optional.

4.4 SIGNAL GROUPS

The ISA bus contains seven groups of signals: address, data, cycle control, central control, interrupt, direct memory access (DMA), and power. The bus signals can support a PRA, which has an onboard DMA controller, optional SRAs, and replying agents providing DMA or I/O memory expansion. The input and output direction designations for each signal are referenced to the PRA.

4.4.1 Address Signal Group

The address signal group consists of signals driven by the requesting agent in order to specify both the addresses and data transfer width.

A(19:0) (I/O)

The A(19:0) (Address) bus signals are latched outputs driven by a requesting agent. They represent the least significant 20 bits of a positive logic binary number, defining a 1M address space. A(19:0) become valid when BUSALE is asserted, and they may be latched by replying agents on the falling edge of BUSALE.

A(19:16) are driven low during I/O cycles. During refresh cycles, the PRA drives A(7:0) with the DRAM row address to be refreshed and drives A(19:8) to 0.

LA(23:17) (I/O)

The LA(23:17) (Unlatched Address) bus signals are driven by a requesting agent. These signals are not latched by the PRA. However, they are valid when BUSALE is asserted, and they may be latched on the falling edge of this signal. LA(23:17) represent bits 17 through 23 of the memory address presented on the bus. LA(23:17) should be used by 16-bit replaying agents in generation of SRDY*, MCS16*, and IOCS16*.

The requesting agent drives LA(23:17) during any transfer cycle. LA(23:17) are driven to 0 during I/O cycles. During Secondary requesting agent cycles, LA(23:17) must be vaid throughout the entire transfer cycle, and BUSALE is asserted by the PRA.

The PRA drives LA(23:17) to 0 during refresh cycles.

SBHE* (I/O)

SBHE* (System Bus High Enable) is asserted by a requesting agent to indicate a transfer of data on lines D(15:8).

BUSALE (O)

BUSALE (Bus Address Latch Enable) is an address strobe driven by the PRA. LA(23:17) are valid when BUSALE is asserted, and they may be latched on the falling edge of BUSALE. A(19:0) are latched by the PRA on the leading edge of BUSALE during bus cycles initiated by the PRA.

All agents must be level sensitive with respect to BUSALE. This means that although the address signal group signals or decodes generated from them may be latched by agents on the falling edge of BUSALE, all agents must monitor the address signal group signals whenever BUSALE is asserted. This is especially important during DMA cycles, Secondary requesting agent cycles, and refresh cycles.

For all DMA controller cycles (including Secondary requesting agent cycles), the PRA asserts BUSALE to allow the LA(23:17) address to "pass through" transparent address latches to the bus.

AEN (O)

AEN (DMA Address Enable) is asserted by the PRA when its CPU is in the hold mode and its DMA controller has control of the ISA bus. AEN is negated by the PRA when its CPU is in control of the ISA bus or when the DMA controller has granted the ISA bus to an SRA. When AEN is asserted, all agents other than the PRA must tri-state their address signal group and cycle control signal group outputs to the ISA bus.

During DMA cycles, the validity of LA(23:17), A(19:0) is indicated by the assertion of both AEN and BUSALE.

SRAs cannot conduct DMA cycles because only the PRA can drive the DACKn* and AEN signals.

4.4.2 Data Signal Group

The data signal group consists of one set of 16 data bits. Data transfers may occur over either of the two bytes independently of one another.

D(15:0) (I/O)

On the D(15:0) (Data Bus), D15 is the most significant bit and D0 is the least significant bit. All 8-bit replying agents must connect only to the least significant eight data lines, D(7:0). To support communication of 8-bit replying agents to 16-bit requesting agents, both data swapping and transfer reformatting are supported by the PRA. During odd-byte transfers between a 16-bit requesting agent and an 8-bit replying agent, the PRA drives the data appearing on D(7:0) onto D(15:8). Transfer reformatting is accomplished by the PRA when it formats 16-bit accesses to 8-bit replying agents as two consecurtive 8-bit ISA bus cycles.

The PRA tri-states D(15:00) during refresh operations.

4.4.3 Cycle Control Signal Group

The cycle control signals control the duration and type of cycles. The group consists of six command signals, two ready signals, and three sinals which specify the cycle type.

The command signals define the address space (memory or I/O) and the data direction (read or write). The ready signals modify the command pulse widths to lengthen or shorten the default cycle timings.

MEMR*, MRDC* (I/O)

MRDC* (Memory Read Command) is asserted when the requesting agent is ready for a replying agent to drive the data bus with the contents of the memory specified by LA(23:17), A(19:0). MEMR* is identical in function to MRDC*, except that it is asserted only when the memory read access falls below 1M. Eight-bit agents will receive only MEMR*.

The refresh circuity on the PRA asserts MEMR* and MRDC* during refresh cycles initiated by an SRA in control of the ISA bus.

MEMW*, MWTC* (I/O)

MEMW* (Memory Write Command) is asserted during a write cycle when the requesting agent is driving the data bus. MEMW* is identical in function to MWTC*, except that it is asserted only when the memory write access falls below 1M. Eight-bit agents receive only MEMW*.

IORC* (I/O)

IORC* (I/O Read command) is asserted when the requesting agent is ready for a replying agent to drive the data bus with the data available from the I/O port specified by A(15:0).

IOWC* (I/O)

IOWC* (I/O Write command) is asserted during an I/O write cycle when the requesting agent is driving the data bus and it is negated when a replying agent ust clock the data into the I/O port specified by A(15:0).

MCS16* (I)

MCS16* (16-bit Memory Cycle Select) is asserted by a 16-bit memory agent to indicate to the requesting agent that a 16-bit cycle may be executed, replying agents generate MCS16* based on a decode of LA(23:17). Timing requirements placed on MCS16* prevent use of the memory command signals MEMR*/MRDC* and MEMW*/MWTC* is generation of MCS16*. The requesting agent ignores MCS16* on I/O cycles.

IOCS16* (I)

IOCS16* (16-bit I/O Cycle Select) is asserted by a 16-bit I/O agent to indicate to the requesting agent that a 16-bit cycle may be executed. Replying agents generate IOCS16* based on a decode of A(15:0). Timing requirements placed on IOCS 16 prevent use of IOWC* and IORC* in generation of IOCS16*. The requesting a gent ignores IOCS16* on memory cycles.

IOCHRDY (I)

IOCHRDY (I/O Channel Ready) is an asynchronous ready signal from a replying agent. It is negated to force the requesting agent to lengthen the bus cycle by inserting an integral number of wait states (one-half of an ISA bus SYSCLK period, or 62.5μs.) IOCHRDY must not be negated for longer than 15μs. IOCHRDY is ignored by the PRA during zero-wait state cycles.

SRDY* (I)

SRDY* (Synchronous Ready) is asserted by the replying agent to terminate the current bus cycle without any further wait states. The absolute minimum command pulse width is nominally 1 SYSCLK period (125ns) in length, and is known as a zero-wait state cycle, SRAs are not required to support SRDY*.

MEMREF* (I/O)

MEMREF* (Memory Refresh) is asserted during a DRAM refresh cycle. By design, only memory read cycles may occur while MEMREF* is asserted. The address present on A(7:0) is used by memory agents as the address of the row to be refreshed.

An SRA may, if it is the current bus owner, tri-state its address, command, and data drivers and asserts MEMREF* to force the PRA to conduct a refresh cycle. SRAs must do this every 15μs if they retain ownership of the ISAS bus, or the contents of the system DRAM will be lost. When a refresh cycle is initiated in this manner, the PRA asserts A(7:0) and MEMR*/MWTC*.

Refresh cycles occur at a period of 15μs. Each of the 256 possible refresh addresses must therefore be refreshed at least once every 4 ms.

4.4.4 Central Control Signal Group

The central control group consists of special timing, control, and error signals. The function of these signals is as follows.

SECMAST* (I)

SECMAST* (Secondary Master) is asserted by an SRA to gain control of the ISA bus after receiving the appropriate DACKn* from the PRA. When SECMAST* is asserted, all other requesting agents must tri-state their address, data, and control signals. After SECMAST* is asserted, the Secondary requesting agent must wait at least one SYSCLK period before driving the address and data group signals, and it must wait at least two SYSCLK periods before driving the cycle control group signals. If SECMAST* is asserted for longer than 15μ, the SRA must initiate refresh cycles to maintain DRAM data integrity. Note that only DMA channels programmed in the cascade mode may be used by SRA's wishing to gain control of the ISA bus.

IOCHCK* (I)

IOCHCK* (I/O Channel Check) may be asserted by any agent to signal an error condition that cannot be corrected, such as a memory parity error. IOCHCK* must be asserted for at least 15μs for the PRA to recognize that an error condition has occured.

RESETDEV (O)

RESETDEV (Reset) is asserted by the PRA to initialize all agents on the ISA bus after power-up or during a low-voltage condition.

SYSCLK (O)

SYSCLK (System Clock) has a frequency of 8MHz with a 50% duty cycle, and it is driven by the PRA. Bus cycle times are directly proportional to the clock period. All synchronous signals on the ISA bus are synchronous to SYSCLK.

Bus cycles are lengthened by IOCHRDY or shortened by SRDY* in integer multiples of one-half the SYSCLK period. For example, SRDY* could be asserted during a 16-bit cycle to reduce the command pulse width to 1.5 SYSCLK periods. Likewise, IOCHRDY could lengthen a 16-bit cycle to N +2.5 SYSCLK periods, where N is the number of wait states that the accessed device requests. Since the DMA controller operates off of a 4MHz clock, DMA cycles are extended in multiples of 2 SYSCLK periods.

80OSC (O)

84OSC (Oscillator Output) is a 50-percent duty cycle clock signal with a frequency of 14.31818MHz. 84OSC is not synchronous to either SYSCLK or any other signals on the ISA bus, so it must not be used in applications which require synchronization to the ISA bus. 84OSC is intended to be used in timing or counting operations only.

4.4.5 Interrupt Signal Group

The interrupt signal group consists of a set of signals that can be used by a replying agent to obtain interrupt service from a requesting agent.

IRQ (I)

Asserting the IRQ (15, 14, 12:09, 07:03) (Interrupt Request) line requests an interrupt. The line must remain asserted until the interrupt is acknowledged by the appropriate software interrupt service routine.

4.4.6 DMA Signal Group

These signals control DMA service and transfer of bus ownership from the PRA to an SRA.

DRQ (I)

DRQ (7:5, 3:0) (Direct Memory Access Request) signals are asynchronous channel requests used to gain either DMA service or control of the ISA bus from the PRA. DMA service or bus control can be attained by asserting DRQ line and keeping it aserted until the corresponding DACKn* line is aserted by the PRA. When SRAs wish to gain control of the ISA bus, they must only use DMA channels that have been programmed to operate in the cascade mode.

DACK* (O)

DACK (7:5, 3:0)* (DMA Request Acknowledge) lines are driven by the PRA to acknowledge DMA requests DRQ (7:5, 3:0). I/O repliers use DMA acknowledge signals for address selection during DMA cycles when AEN is asserted.

TC (O)

TC (Terminal Count) is asserted by the PRA when any one of its DMA channels has reached its terminal count, signalling the end of the pre-programmed DMA transfer.

4.4.7 Power Signal Group

The ISA bus provides DC power at +5 volts, −5 volts, +12 volts, −12 volts, and 0 volts (Ground).

+5 VOLTS

Three pins supply current for 16-bit agents. Two (2) pins supply current for 8-bit agents.

−5 VOLTS

One pin supplies current.

+12 VOLTS

One pin supplies currents.

-12 VOLTS

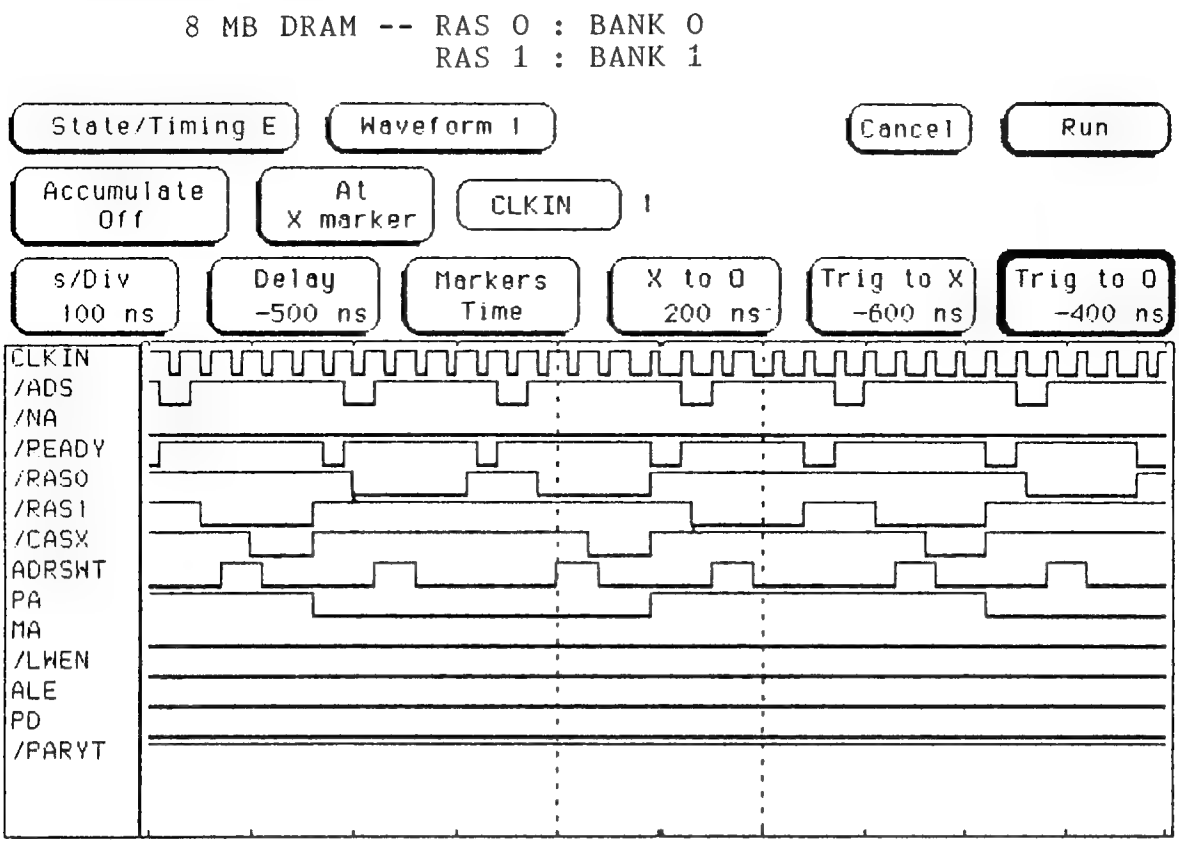
One pin supplies current.

0 VOLTS (GROUND)

Four pins provide a return path for the current supplied by the other power pins for 16-bit agents. Three pins provide this return path for 8-bit agents.

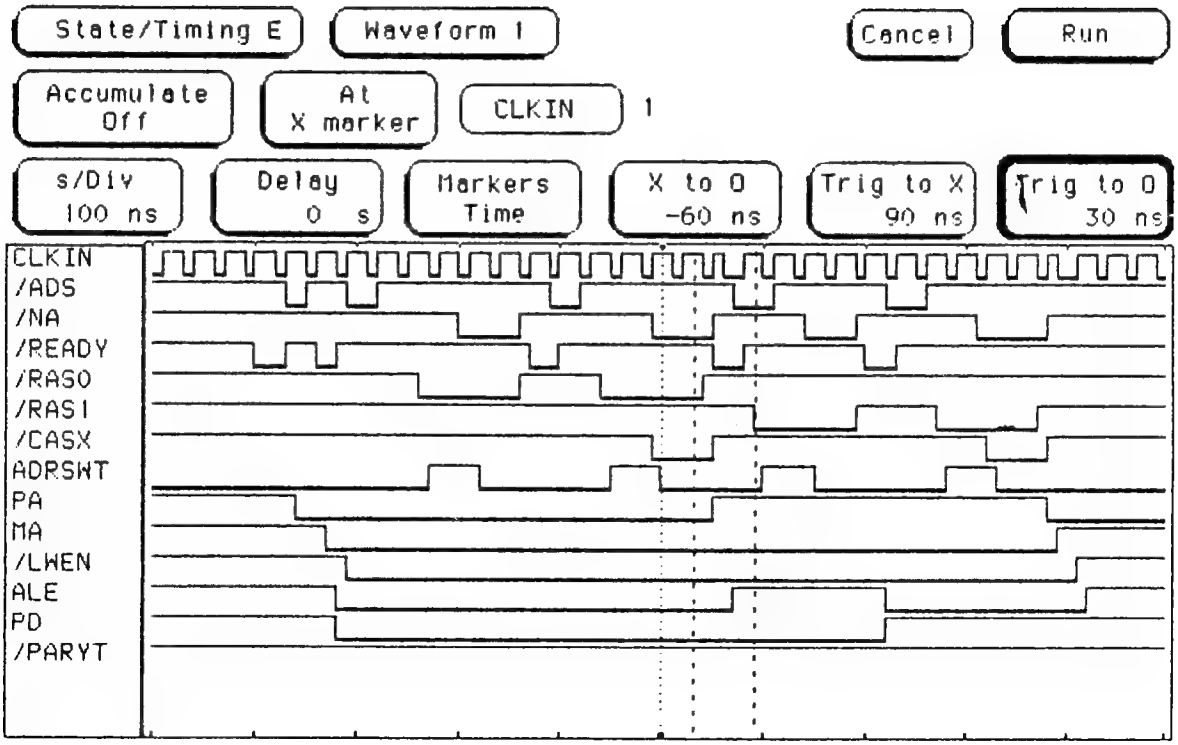
4.5 KEY POINTS TIMING CHART

4.5.1 Interleaved Dram Timing




```
RAS  DELAY   :  1 CLKINS
CAS  DELAY   :  2 CLKINS
CAS ACTIVE   :  2 CLKINS
RAS PRECHARGE : 4 CLKINS
RECOVERY TIME : 0 CLKINS
```

4.5.2 Interleaved Dram Timing 2



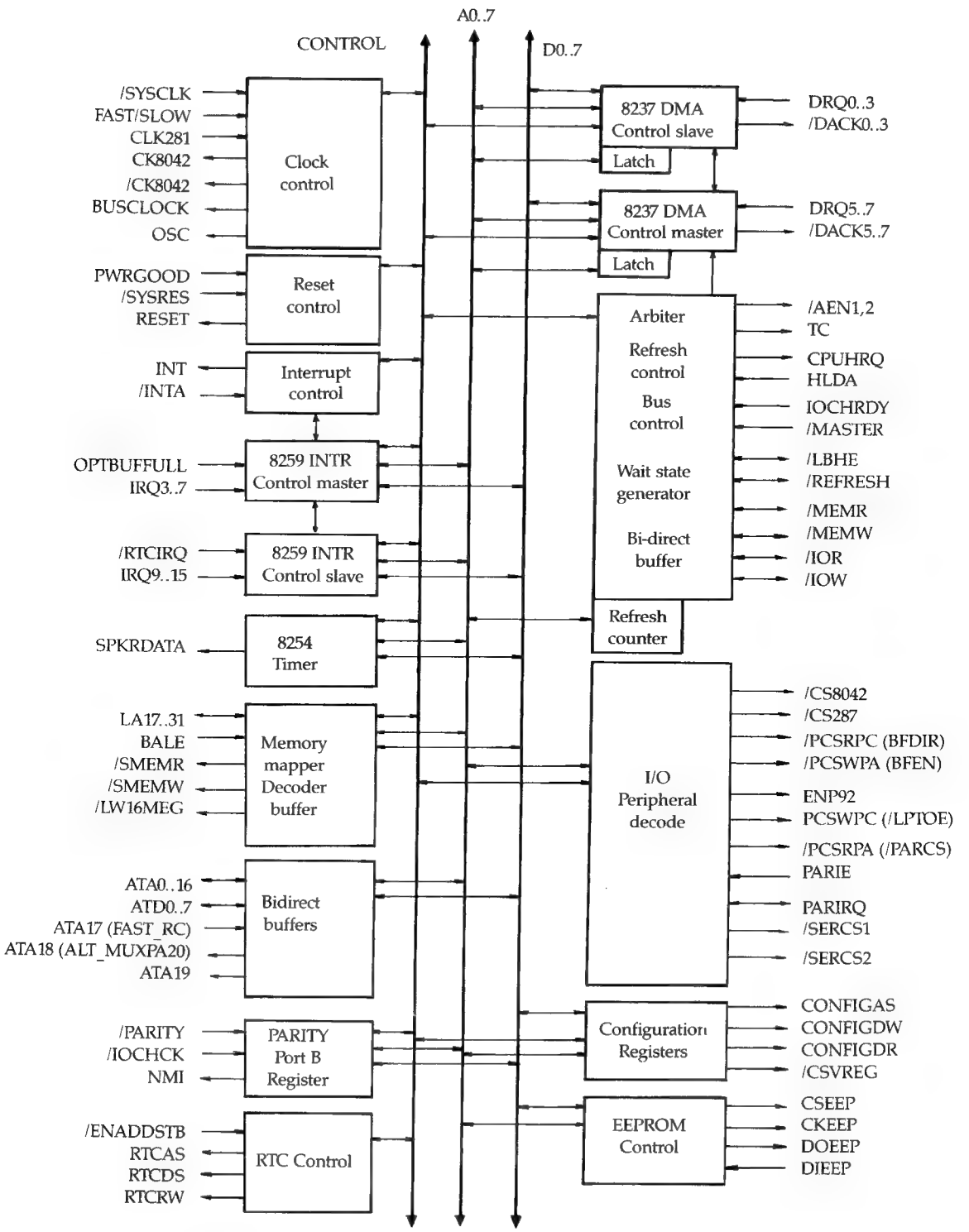
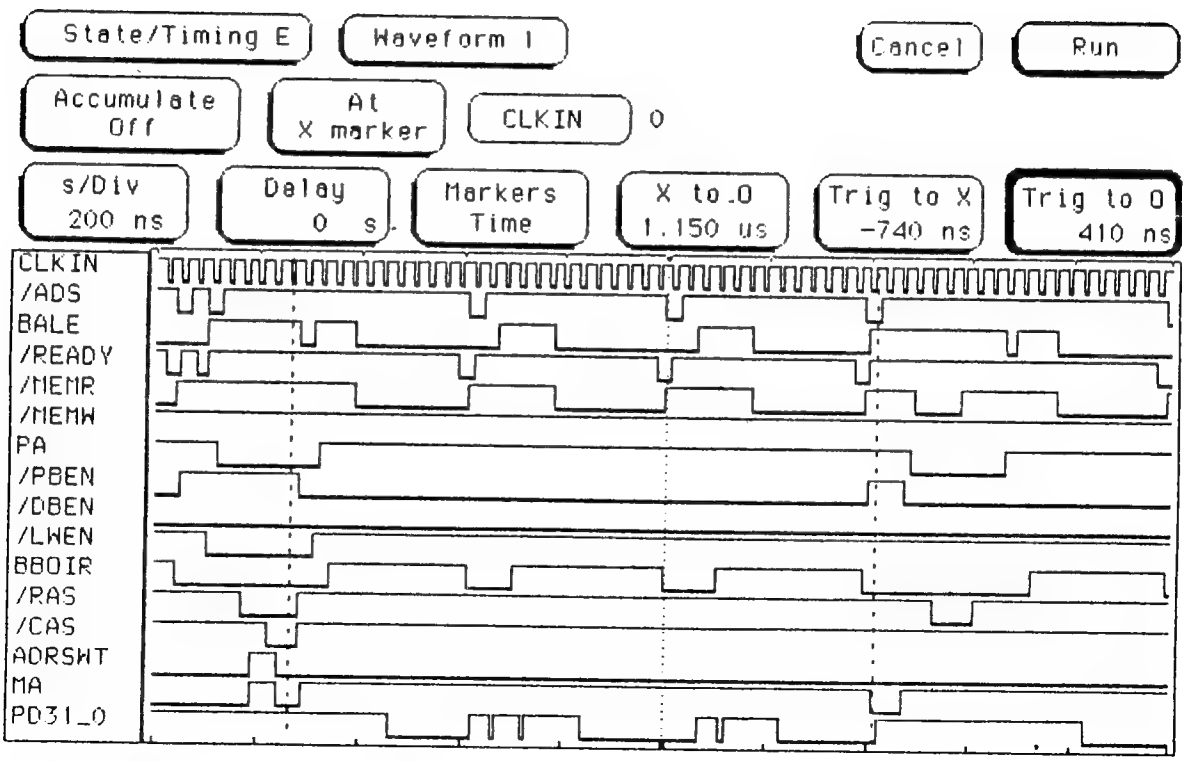


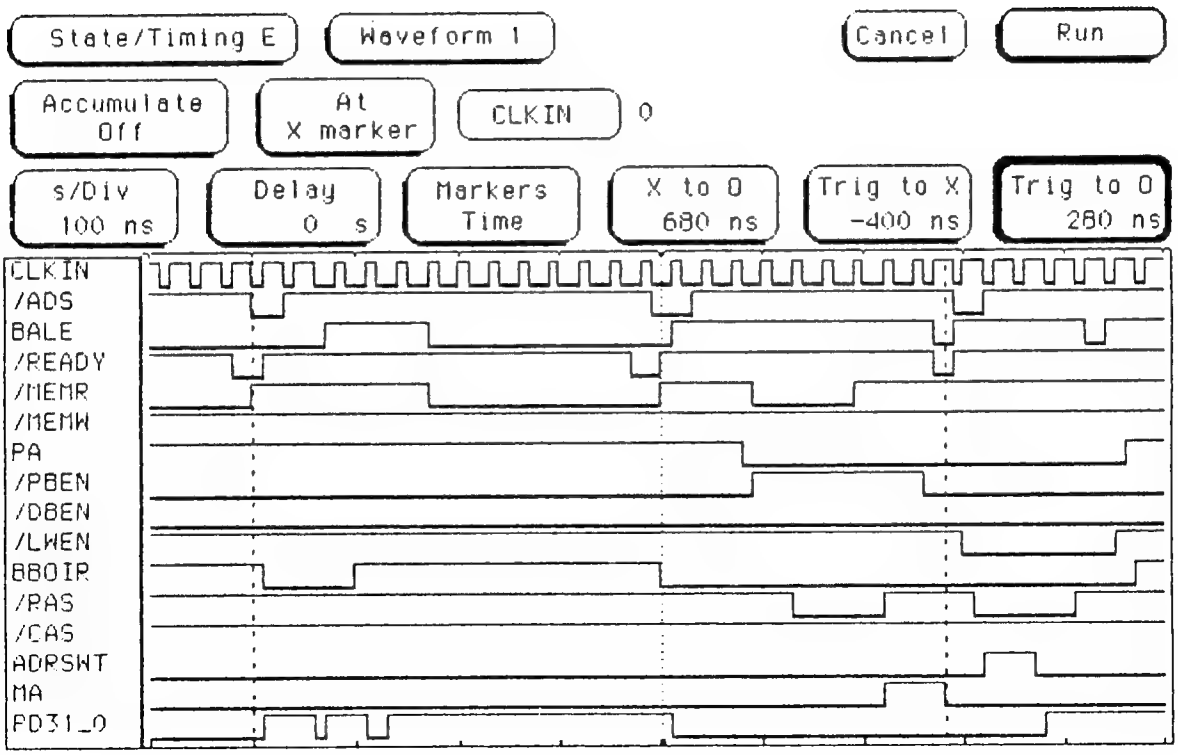
Figure 5-1. GC131 Peripheral Controller Block Diagram

4.5.3 Non-Interleaved Dram Timing 1

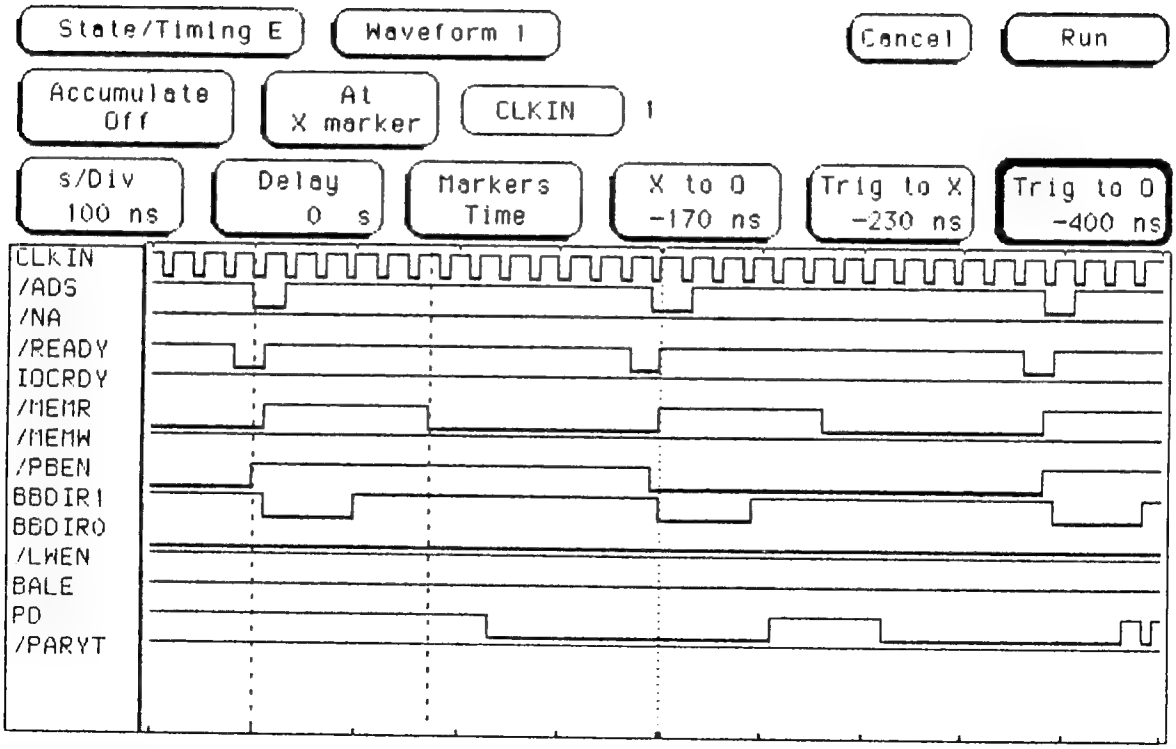



```
RAS DELAY     : 3 CLKINS
CAS DELAY     : 3 CLKINS
CAS ACTIVE    : 8 CLKINS
RECOVERY TIME : 2 CLKINS
RAS PRECHARGE : 8 CLKINS
```

4.5.4 Non-Interleaved Dram Timing 2

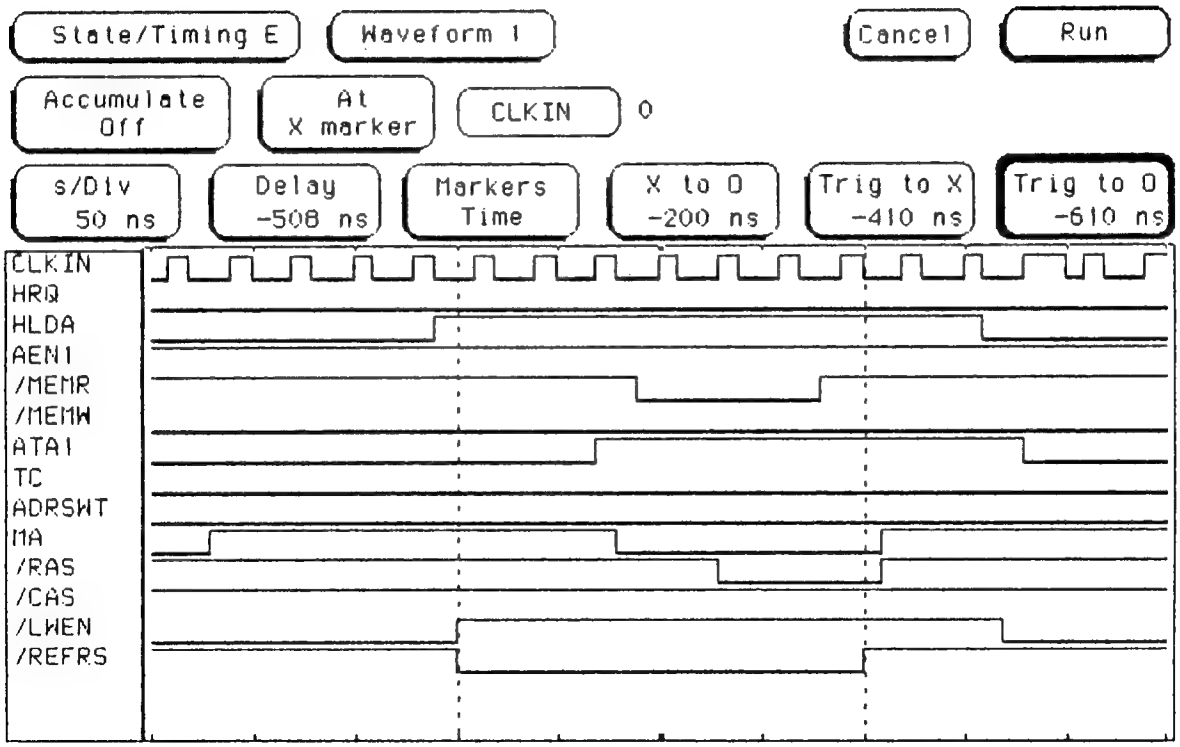


4.5.5 16 Bits Access to 16 Bits OFF B'D Dram



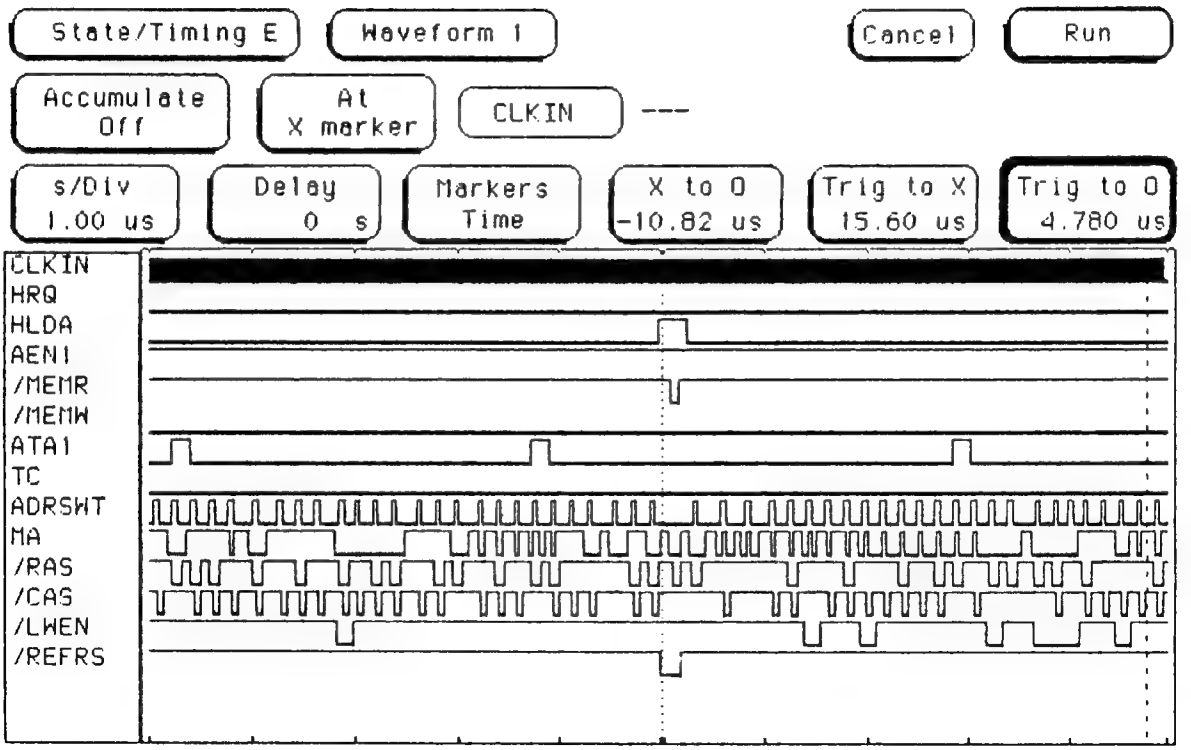
COMMAND DELAY : 7 CLKINS
COMMAND ACTIVE : 13 CLK INS
RECOVERY TIME : 6 CLKINS

4.5.6 Refresh Timing

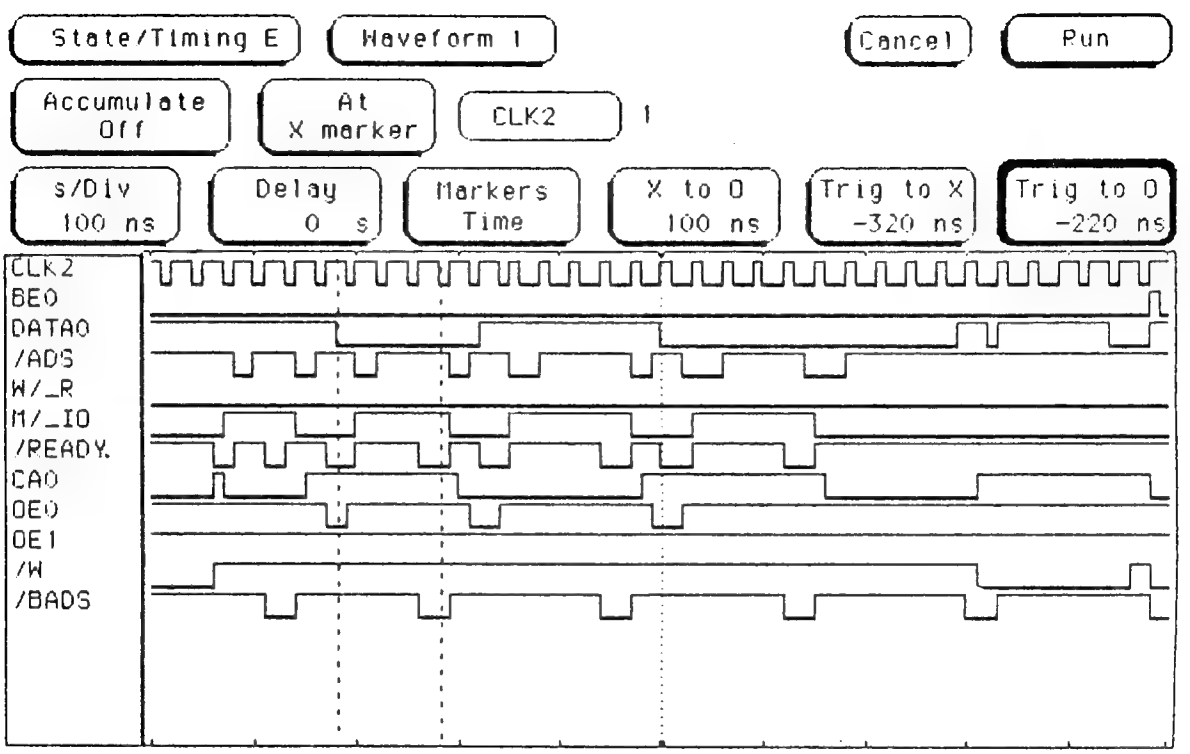


SPEED FAST
REFRESH CLOCK : DIVIDED BY 4
WAIT STATE : 0

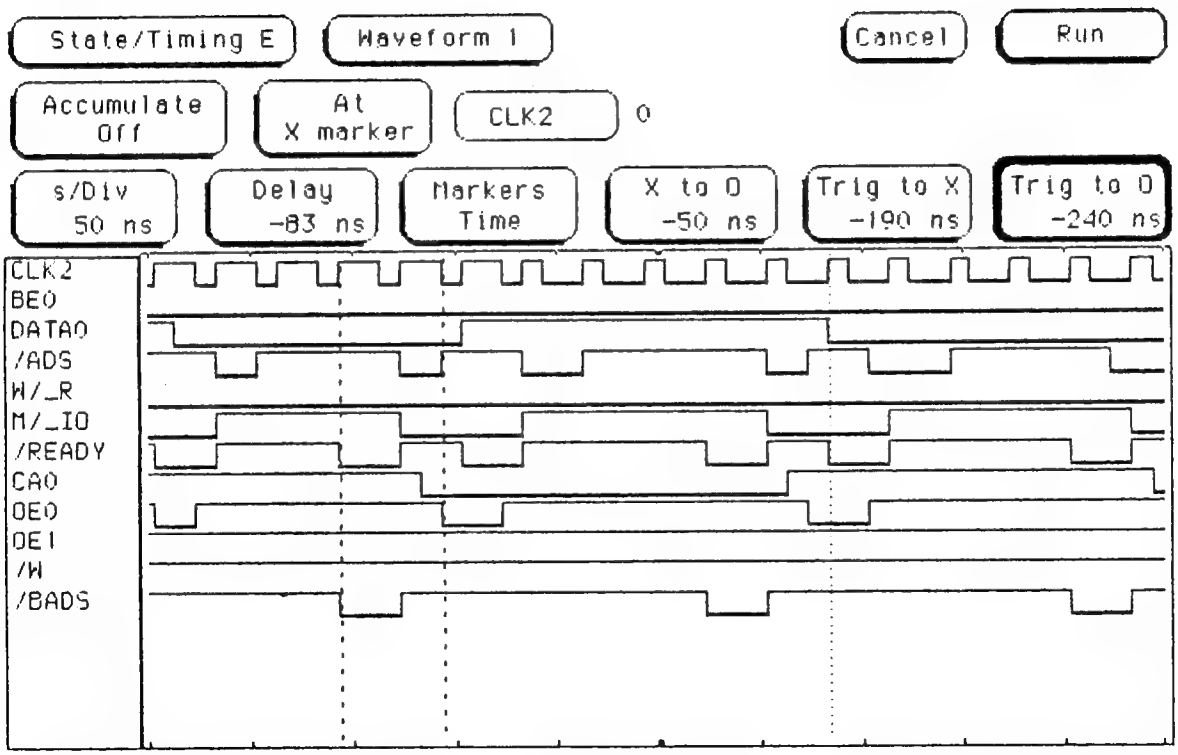
4.5.7 Refresh Timing 2



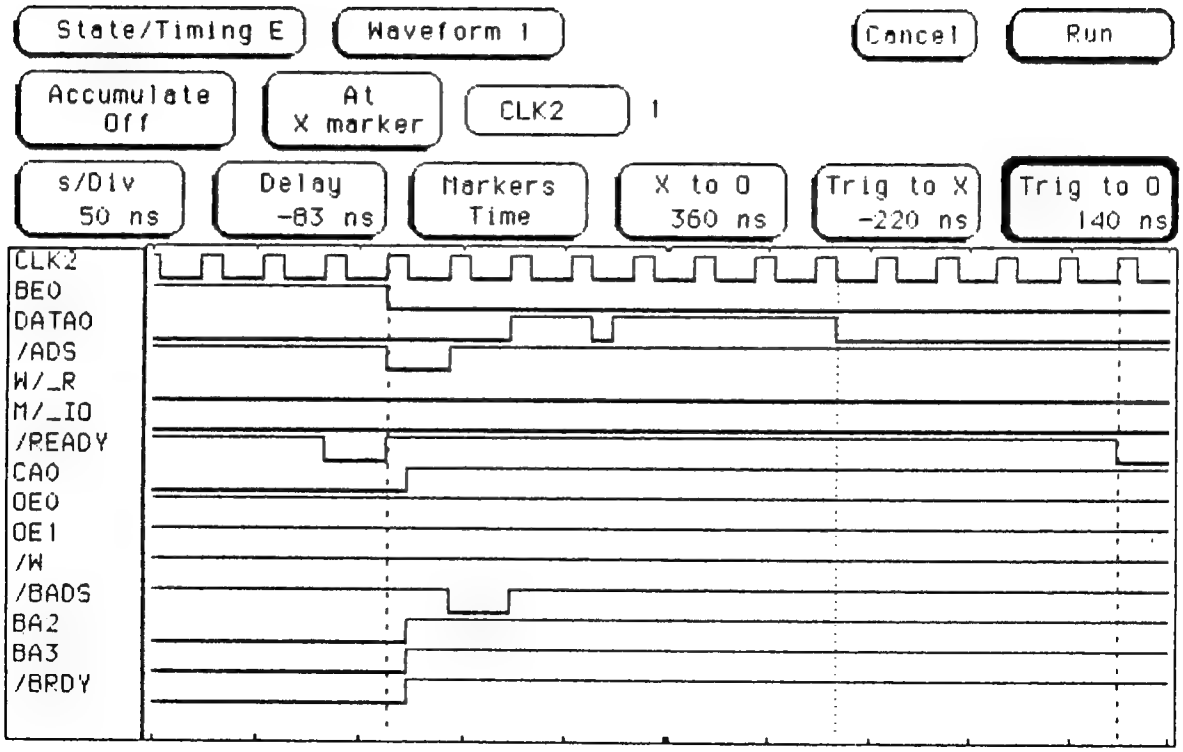
4.5.8 Cache Hit Cycle



4.5.9 Cache Hit Cycle 2



4.5.10 Cache Miss Cycle



5

GC131 PERIPHERAL CONTROLLER

5.1 INTRODUCTION

This Chapter provides an overview of the GC131 Peripheral controller and describes the detailed function of all components which are contained in this chip.

5.2 GC131 PERIPHERAL CONTROLLER OVERVIEW

This single chip contains many components and effectively takes the place of them. These components are as follows:

- A 8254 programmable interval timer (PIT)
- Two 8259 programmable interrupt controllers (PICs)
- Two DMA controllers
- An LS612 and other devices

The GC121 Peripheral Controller block diagram (Figure 5-1) shows the range of services provided by this chip. The GC131 Controller is responsible for the AT controllers of the chip set supporting the system with INTERRUPT, TIMER, DMA/REFRESH, and I/O services.

5.2.1 HT131 Peripheral Controller Pinouts

The pin connections for the *HT131 Peripheral Controller* are shown in Figure 5-2. The pins are numbered sequentially in a counter-clockwise direction from the index mark as viewed from the botton of the chip.

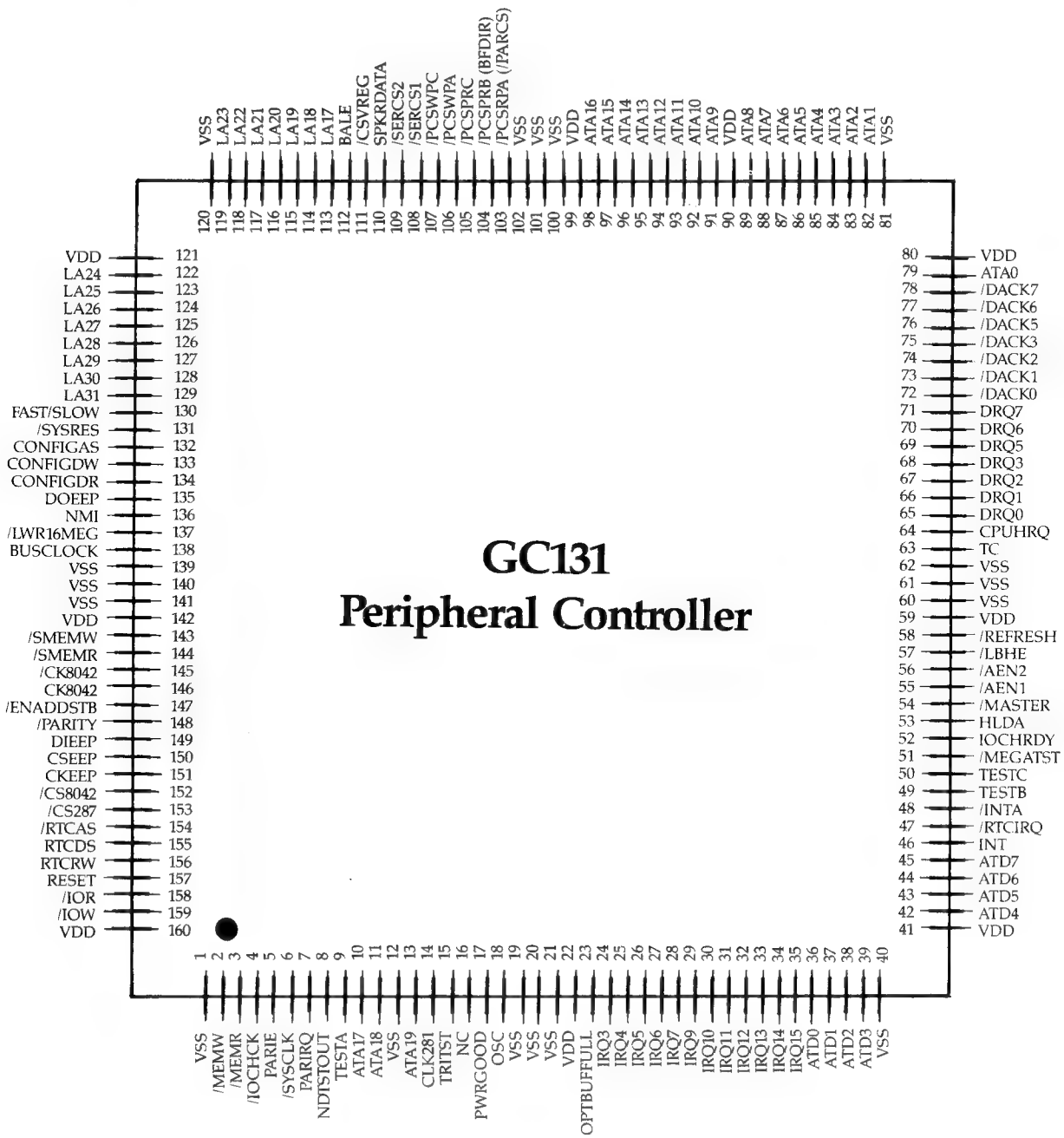


Figure 5-2. HT131 Peripheral Controller Pinouts

5.2.1 HT131 Peripheral Controller Pinouts

The pin connections for the *HT131 Peripheral Controller* are shown in Figure 5-2. The pins are numbered sequentially in a counter-clockwise direction from the index mark as viewed from the botton of the chip.

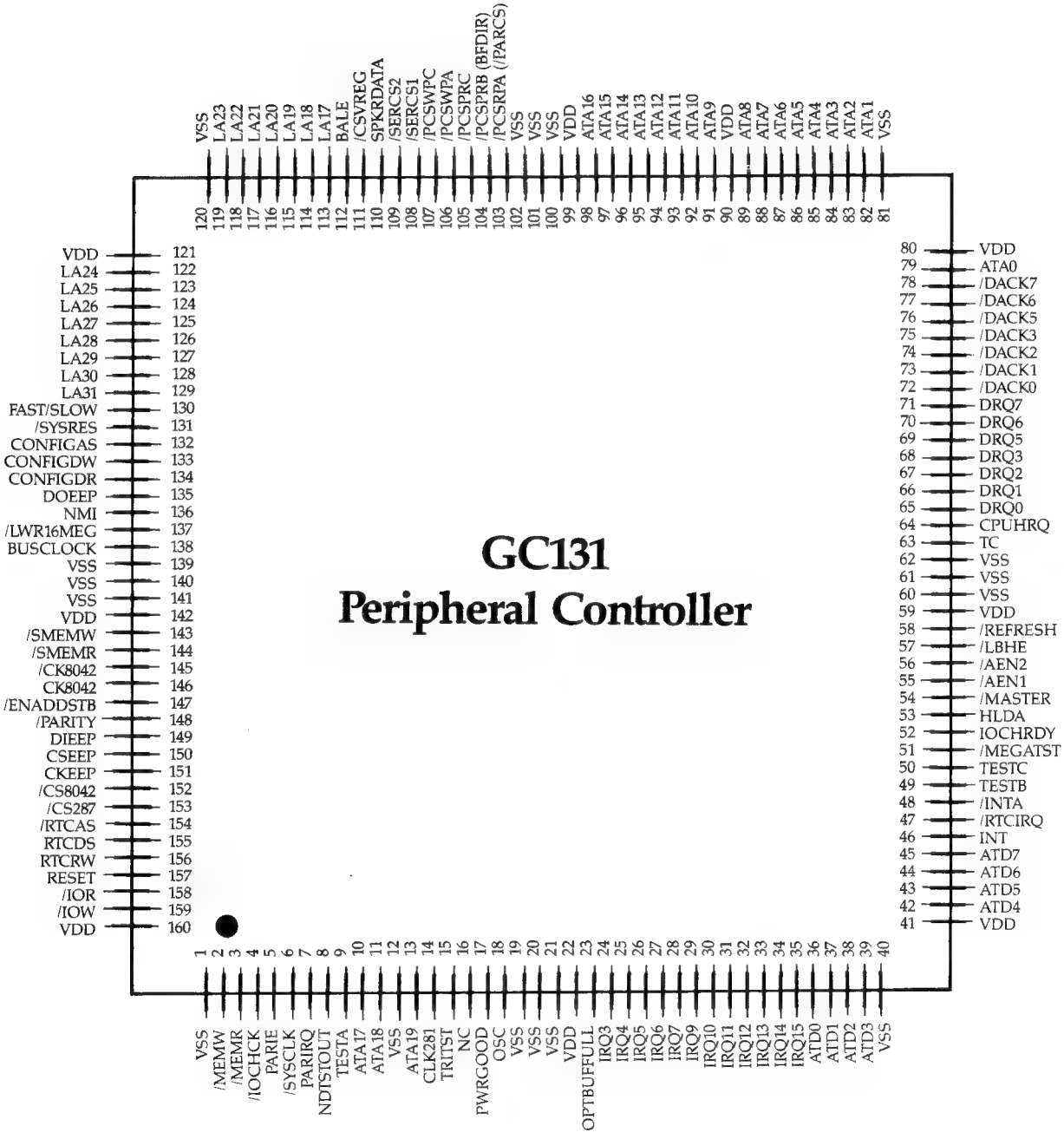


Figure 5-2. HT131 Peripheral Controller Pinouts

5.2.2 HT131 Peripheral Controller Pin Descriptions

This section describes the pins of the *HT131 Peripheral Controller*. The pin identification numbers correspond with those shown in *"Figure 5-2 - HT131 Peripheral Controller, pinouts"*.

Pin Symbol	Pin Number	Pin Type	Description
/AEN1	55	O	**Address Enable** (DMA Controller - 1). When active /AEN1 indicates that the system is performing an 8-bit DMA transaction.
/AEN2	56	O	**Address Enable** (DMA Controller - 2). When active /AEN2 indicates that the system is performing a 16-bit DMA transaction.
ALT-MUXPA20	11	O	(Redfined from ATA18). When the PORT92h feature is enabled (See *PORT 92H* on Page 78), this ALT-MUXPA20 signal should be gated with the MUXPA20 signal from the 8042 Keyboard Controller to produce the final MUXPA20 signal that is sent to the *HT132 Controller.* (See also *INDEX 48h* and cicuitry shown on Page 76).
ATA0 to ATA16	79, 82-89, 91-98	I/O	**Latched AT Address Bus:** Used for memory and I/O devices. These addresses are gated from the system bus when BALE is set HIGH, and are latched on the falling edge of BALE. These signals are generated by the CPU or DMA controller (in the *HT131 Controller),* or may be driven by an external bus master on the I/O channel.
ATA17	10	O	**AT Address Line 17.** Pin 10 can be redefined to either of two modes. In I/O Standard Mode the line ATA17 is driven only during DMA and REFRESH cycles and represent a copy of LA17. In I/O PORT92h Mode, Pin 10 is refined as FAST-RC-as described later in these *Pin Descriptions.* (See also *PORT 92H* on Page 78.)

Pin Symbol	Pin Number	Pin Type	Description
ATA18	11	O	**AT Address Line 18.** Pin 11 can be redefined to either of two modes. In I/O Standard Mode the line ATA18 is driven only during DMA and REFRESH cycles and represent a copy of LA18. In I/O PORT92h Mode, this pin is refined as ALT-MUXPA20-as described later in these *Pin Descriptions.* (See also *PORT 92H* on Page 78).
ATA19	13	O	**AT Address Line 19.** This line is driven only during DMA and REFRESH cycles and represent a copy of LA19.
ATD0 to ATD7	36-39, 42-45	I/O	**AT Data bus**, LOW byte. The *HT131* uses only 8-bit transfers for accessing its internal registers.
BALE	112	I	**Buffered Address Latch Enable:** Connects with the *HT132* 'BALE' line. Used to latch valid addresses and memory decodes from the CPU. It indicates valid CPU or DMA address for the I/O channel. BALE is HIGH during 'Hold Acknowledge DMA', 'REFRESH' or 'MASTER' cycles.
BFDIR	104	O	[Redefined from /PCSRPB] **On-Board I/O Data Buffer Directional Control;** used when the **16C452 Interface Mode** (that allows connection to discrete parallel ports of the 16C452 Interface) is enabled by setting Bit 0 of INDEX48h (See *'INDEX48h'* on Page 74.
/BFEN	106	O	[Redefined from /PCSWPA] **On-board I/O Data Buffer Enable;** used when the 16C452 Interface Mode is enabled.
BUSCLOCK	138	O	**Bus Clock** drives the backplane clock signal whose frequency is divided by the value set in the configuration register and output on this line. (*See 'INDEX40h' and 'INDEX41h'* on Page 65).

Pin Symbol	Pin Number	Pin Type	Description
CK8042	146	O	**Clock Driver Phase 1** (Frequency = 7.16 or 11.5 MHz): Connects with the Keyboard Controller clock input. The signal on pin CLK281 is divided by four. (See *'INDEX48h'* on Page 74 and the setting of Bit 2 that changes the frequency of CK8042)
/CK8042	145	O	**Clock Driver Phase 2:** 180° out of phase with CK8042.
CKEEP	151	O	**Clock for EEPROM** (NVRAM).
CLK28I	14	I	**Clock 28 In** (Frequency = 28.6363MHz): At twice the Backplane OSC frequency the oscillator is used to drive the internal timers and the Keyboard Controller oscillator.
CONFIGAS	132	O	**Configuration Registers Address Strobe:** On the triling edge of this signal, data is latched into the *HT131, HT132* and *HT133* index registers.
CONFIGDR	134	O	**Configuration Registers Data Read:** When active and selected by the INDEX value (within an appropriate range), and of the *HT131, HT132, HT133 Controllers* will output the indexed value onto the data bus.
CONFIGDW	133	O	**Configuration Registers Data Write:** When active and selected by the INDEX value (within an appropriate' range), one of the *HT131, HT132, HT133 Controllers* will latch in the data to the indexed register on the trailing, edge of this signal.
CPUHRQ	64	O	**CPU Hold Request:** Connects with the 80386 Microprocessor HOLD pin.
/CS287	153	O	**Chip Select for 80287/80387:** When active /CS287 indicates that the processor is accessing the coprocessor I/O in the range F0h to FFh.

Pin Symbol	Pin Number	Pin Type	Description
/CS8042	152	O	**Chip Select** for the 8042 Keyboard Controller.
CSEEP	150	O	**Chip Select** for EEPROM (NVRAM): Used to save the last selected configuration register values.
/CSVREG	111	O	**Video Configuration Register Write strobe.** (See *"Index Address 44h'* on Page 70).
/DACK0 to /DACK3, /DACK5 to /DACK7	72-78	O	**DMA Acknowledge:** When active indicates that the device requesting DMA now has service and can remove its DMA request (DRQ).
DIEEP	149	I	**Data Input for EEPROM** (NVRAM): Connects directly with the EEPROM 'data out' line.
DOEEP	135	O	**Data Output for the EEPROM** (NVRAM).
DRQ0 to DRQ3, DRQ5 to DRQ7	65-71	I	**DMA Requests:** Priorities descrease from DRQ0 to DRQ7. A request is generated by driving a 'DRQ' line HIGH until the corresponding '/DACK' line goes LOW. DRQ0 to DRQ3 perform 8-bit transfers, and DRQ5 to DRQ7 perform 16-bit transfers.
/ENADDSTB	147	I	**Enable Address Strobe on the Real-Time Clock:** When active it prevents any accesses to or from the Real Time Clock.
ENP92	16	O	**Enable PORT 92h.** Used in conjunction with INDEX 48h, Mode Reconfiguration Register (Bit 1), the status of ENP92, when HIGH confirms that the PORT92h feature is enabled. (See also *INDEX 48h* and cicuitry shown on Page 76).
FAST-RC	10	O	[Redefined from ATA17] **Fast RC Reset** is active HIGH. A 110 to 135μs pulse to be gated externally with the 'RC' line from the 8042 Keyboard Controller and presented to the *HT132 CPU/Memory Controller*. (See also *INDEX 48h* and cicuitry shown on Page 76).

Pin Symbol	Pin Number	Pin Type	Description
FAST/SLOW	130	I	**FAST/SLOW clock speed select** from 8042 Keyboard Controller. SLOW indicates a 7MHz clock speed, and FAST indicates 33MHz.
HLDA	53	I	**Hold Acknowledge:** Indicates that the CPU is no longer driving the buses. Used in the DMA controller section.
INT	46	O	**Interrupt Request** to the CPU, from the 8259 Interrupt controller in the *HT131 Controller*.
/INTA	48	I	**Interrupt Acknowledge:** Decoded from 'CPU STATUS' by the *HT132 Controller,* /INTA instructs the *HT131 Controller* to place the interrupt vector (to the CPU) on the system data bus.
/IOCHCK	4	I	**I/O Channel Check:** When active the backplane is indicating that a PARITY check occurred on a backplane memory board.
IOCHRDY	52	I	**I/O Channel ready:** When LOW the current cycle is extended (in multiples of the CLOCK signal) until IOCHRDY is released. IOCHRDY will extend CPU, DMA and REFRESH cycles.
/IOR	158	I/O	**I/O Read:** Normally an input, except during a DMA but not a MASTER, it is driven by the DMA Controller.
/IOW	159	I/O	**I/O Write:** Normally an input, except during a DMA but not a MASTER, it is driven by the DMA controller.
IRQ3 to IRQ7, IRQ9 to IRQ15	24-35	I	**Interrupt Requests:** Interrupts from the I/O channel, indicate that an external peripheral on the backplane is requesting service by the CPU. These inputs are used by the 8259 Interrupt Controller in the *HT131 Controller.* Priorities decrease from IRQ9 to IRQ15, and then from IRQ3 down to IRQ7. An interrupt request is generated on the rising edge of an "IRQ" line — which must be held HIGH until acknowledged by the interrupt service routine.

Pin Symbol	Pin Number	Pin Type	Description
LA17 to LA31	113 to 119, and 112 to 129	I/O	**I/O Buffered (unlatched) Processor Address bus:** Used for memory and I/O devices. LA17 to LA23 are used in AT implementation, to provide addressing up to 16 Mb. They are valid only when BALE is HIGH. These signals are generated by the CPU or the DMA controller (in the *HT131 Controller*), or they may be driven by an external bus master on the I/O channel. In the AT implementation, the unused addresses (LA24 through LA31) must be connected through resistors to ground.
/LBHE	57	I/O	**Bus High Enable:** When active /LBHE indicates that data is valid on the upper half of the AT data bus. Normally this signal is an input-except during DMA when it is driven by the DMA controller; but, during MASTER cycles, /LBHE is driven from the back-plane and is therefore an input.
/LPTOE	107	O	[Redefined from /PCSWPC] **Line Printer Output Enable;** used when the **HT16C452 Interface Mode** (that allows connection to discrete parallel ports of the HT16C452 Interface) is enabled by setting Bit 0 of INDEX48h (See *'INDEX48h'* on Page 74.
/LW16MEG	137	O	**Lower 16 Mb Address:** This signal is not used in the AT implementation. Indicates address is in the lower 16 Mb of memory.
/MASTER	54	I	**Master Mode request:** When active the peripheral device on the backplane is requesting that it become the SYSTEM MASTER, where it will drive the 'adress', 'command', 'refresh' and 'data' lines. The device may drive /REFRESH to request a REFRESH cycle.
/MAGATST	51	I	**Factory Test Pin:** Normally connected to VDD.

Pin Symbol	Pin Number	Pin Type	Description
/MEMR	3	I/O	**Memory Read:** Normally an input - except during DMA when the DMA controller will drive it - this signal is generated by the *HT131 Controller* (for CPU bus cycles), by the *HT131 Controller* (for DMA cycles), or by an external bus master on the I/O channel. It is also generated by the *HT131 Controller* for refresh cycles.
/MEMW	2	I/O	**Memory Write:** Normally an input - except during DMA when the DMA controller will drive it - this signal is generated by the *HT132 Controller* (for CPU bus cycles), by the *HT131 Controller* (for DMA cycles), or by an external bus master on the I/O channel.
NDTSTOUT	8	O	**Factory Test Pin.** To be left unconnected.
NMI	136	O	**Non-Maskable Interrupt** to the 80386: A request to the CPU for immediate service. This signal is generated by /PARITY or /IOCHCK. It is enabled by bit 7 of the NMI Mask register. /PARITY and /IOCHCK are individually enabled by bits in the Port B register of the *HT131 Controller*.
OSC	18	O	**Oscillator** (Frequency = 14.31818MHz): Four-timer the color-burst frequency to the backplane.
OPTBUFFULL	23	I	**Keyboard Output Buffer Full:** Interrupt request from the 8042 Keyboard Controller. This is used as IRQ1 to the 8259 Interrupt Controller in the *HT131 Controller*.
/PARCS	103	O	[Redefined from /PCSRPA] **On-board Parallel Port Chip Select** used when the **HT16C452 Interface Mode** (that allows connection to discrete parallel ports of the HT16C452 Interface) is enabled by setting Bit 0 of INDEX48h (See *'INDEX48h'* on Page 74.

Pin Symbol	Pin Number	Pin Type	Description
PARIE	5	I	**Parallel Port Interrupt Enable** from the printer control register implemented on the system board. **Note:** When using the HT16C452 Interface, this pin must be tied to VCC. The **HT16C452 Interface Mode** (that allows connection to discrete parallel ports of the HT16C452 Interface) is enabled by setting Bit 0 of INDEX48h (See *'INDEX48h'* on Page 74.
PARIRQ	7	I	**Parallel Port Interrupt Request** from a printer. A configuration register *(See 'INDEX43h' on Page* 68) allows enabling and the direction of this interrupt to either IRQ7 (for Port 1) or IRQ5 (for Port 2).
/PARITY	148	I	**Memory Parity Error** from HT132, sampled one '/SYSCLOCK' cycle after the MEMR command.
/PCSRPA	103	O	**Parallel Port Printer Data Read** strobe.
/PCSRPB	104	O	**Parallel Port Printer Status Read** strobe.
/PCSRPC	105	O	**Parallel Port Printer Control Register Read** strobe.
/PCSWPA	106	O	**Parallel Port Printer Data Write** strobe.
/PCSWPC	107	O	**Parallel Port Printer Control Register Write** strobe.
PWRGOOD	17	I	**Power Good:** Indicates that the power levels are ready and stable. The machine is held in 'reset' until PWRGOOD is active. This signal must become active before RESET goes inactive.
/REFRESH	58	I/O	**Refresh Cycle for DRAMs:** Indicates the DMA cycle is actually a 'REFRESH' cycle.
RESET	157	O	**System Reset:** When active the system is in a 'reset state.

Pin Symbol	Pin Number	Pin Type	Description
RTCAS	154	O	**Real-Time Clock Address Write** strobe.
RTCDS	155	O	**Real-Time Clock Data Read** strobe.
/RTCIRQ	47	I	**Real-Time Clock Interrupt Request:** Used as /IRQ8 to the Interrupt Controller in the *HT131 Controller.* It is active LOW.
RTCRW	156	O	**Real-Time Clock Data Read/Write** strobe.
/SERCS1	108	O	**Chip Select for Serial Port 1:** Implemented on the system board.
/SERCS2	109	O	**Chip Select for Serial Port 2:** Implemented on the system board.
/SMEMR	144	O	**Memory Read** command for addresses within the low 1 Mb provided for the I/O channel.
/SMEMW	143	O	**Memory Write** command for addresses within the low 1 Mb provided for the I/O channel.
SPKRDATA	110	O	**Speaker Output** signal to a transistor driving a speaker. It is generated by Counter 2 of the 8254 Timer function and gated by bit 1 of Port B register in the *HT131 Controller*.
/SYSCLK	6	I	**Main HT131 System Clock:** Connects with the *HT132 Controller's* /SYSCLK. The '/SYSCLK' frequency is half that of the CPU 'CLK2'.
/SYSRES	131	I	**System Reset:** Derived from VCC and the RESET pushbutton. /SYSRES is LOW while VCC is LOW, or while the pushbutton is pressed, and goes HIGH after a debounce period. The debounce period should not end while PWRGOOD is still LOW.

Pin Symbol	Pin Number	Pin Type	Description
TC	63	O	**Terminal Count** from the DMA controllers in the *HT131 Controller* to the device on the I/O channel that is doing the current DMA cycle – indicating that this is the last transfer for this DMA channel.
TESTA	9	I	**Factory test pin.** Always connect to ground.
TESTB	49	I	**Factory test pin.** Always connected to ground.
TESTC	50	I	**Factory test pin.** Always connected to ground.
TRITST	15	I	Factory test pin. Always connected to ground.
VDD	22, 41, 59, 80, 90, 99, 121, 142, 160		+5 volts
VSS	1, 12 19, 20, 21, 40, 60, 61, 62, 81, 100, 101, 102, 120, 139, 140, 141		Ground

5.2.3 I/O Address Map

Table 5-1. I/O Address Map

Address range	Device	Operation
0h – Fh	DMA Controller 1 (8237), slave	Read/Write
20h – 21h	Interrupt controller 1 (8259), master	Read/Write
24h	Configuration register – Address	Write only
28h	Configuration register – Data	Read/Write
40h – 43h	Timer/Counter (8254)	Read/Write
60h, 64h	Keyboard Controller (8042)	Chip select
61h	Port Bregister, PPI (8255)	Read/Write
70h	Real-time Clock register – Address, NMI Mask Bit	Write only
71h	Real-time Clock register – Data	Read/Write
80h – 8Fh	DMA Memory Mapper (Page registers)	Read/Write
92h, 93h, 97h, 99h, 9Ah, 9Bh, 9Fh	DMA Memory Mapper (Page registers)	Read/Write
A0h – A1h	Interrupt controller, slave (8259)	Read/Write
C0h – CFh	DMA controller 2 (8237), master	Read/Write
E0h – FFh	Numeric Coprocessor (80287)	Chip select
278h – 27Fh	Parallel Port 2 (Printer)	Read/Write
2F8h – 2FFh	Serial Port 2	Chip select
378h – 37Fh	Parallel Port 1 (Printer)	Read/Write
3F8h – 3FFh	Serial Port	Chip select

Note: Access to these devices is disabled for addresses above 1 Kb and during. DMA operations.

5.2.4 Port B (8255) PPI Register, Address 61h

Data written	
Bit 3 = 1	Disable NMI for IOCHCK(*)
Bit 2 = 1	Disable NMI for Memory PARITY error
Bit 1	Speaker data
Bit 0 = 1	Enable Timer (8254) for speaker
Data read back	
Bit 7 = 1	Memory PARITY error
Bit 6 = 1	IOCHCK error(*)
Bit 5	Timer 2 (8254), output
Bit 4	REFRESH detect
Bit 3 = 1	NMI disabled
Bit 2 = 1	NMI disabled for memory PARITY error(*)
Bit 1	Speaker data
Bit 0 = 1	Timer 2 (8254) for speaker enabled

Note: (*) The default setting on RESET is 00h.

5.2.5 NMI Mask Register, Address 70h

Bit 7 = 1	Disable NMI (Default setting on RESET).
Bit 7 = 0	Enable NMI.

5.2.6 DMA Memory Mapper (Page Registers)

Operation	Mapping Address A16h – 23h	Mapping Address A24h – 31h
/DACK0	87h	97h
/DACK1	83h	93h
/DACK2	81h	91h
/DACK3	82h	92h
/DACK5	8Bh	9Bh
/DACK6	89h	99h
/DACK7	8Ah	9Ah
REFRESH	8Fh	9Fh

Note:
- Twenty-three 8-bit registers between 80h and 9Fh can be written and read back.
- If 8-bit mapping is selected in the configuration register then A2h to A3h produce '00' and no access is allowed to the registers at 90h to 9Fh.
- The mapping addresses are, during DMA and REFRESH cycles, driven on ATA16 to ATA19 and also on LA17 to LA31.

6

GC132 CPU/MEMORY CONTROLLER

6.1 INTRODUCTION

This chapter describes the function and structure of GC132 CPU/Memory controller.

6.2 GC132 CPU/MEMORY CONTROLLER OVERVIEW

This powerful chip decodes the processor address and control lines and generates the RAS, CAS, and chip select signals required for memory management. Both static and dynamic memories can be used. The GC132 Controller features both paged and interleaved memory access techniques that improve overall system throughput.

The GC132 CPU/Memory Controller block diagram (Figure 6-1) shows the range of services provided by the chip. These services, which are used in the control of the CPU and memory, include timing, synchronization, addressing, parity, bus conversion, and AT bus module.

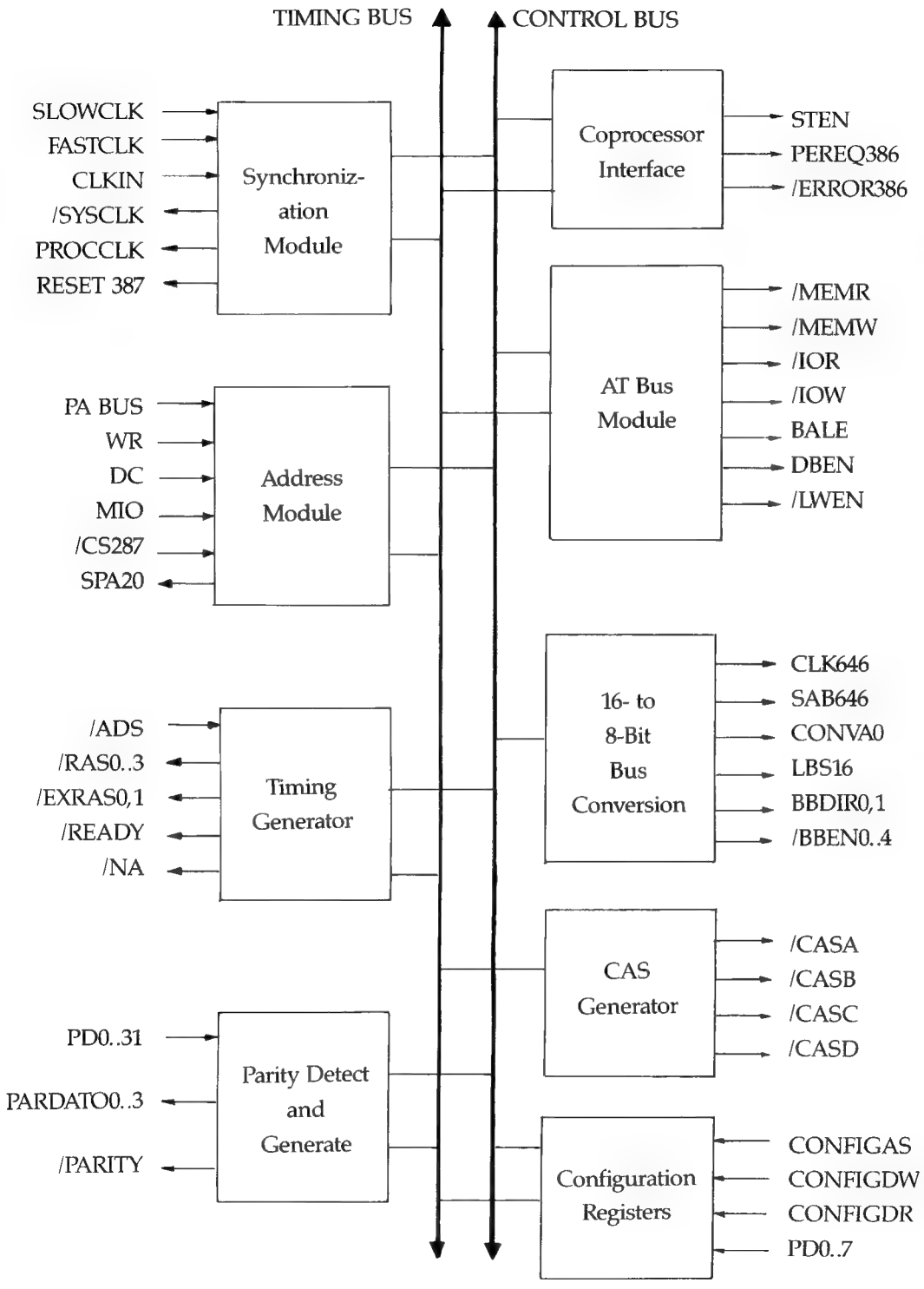


Figure 6-1. GC132 CPU/Memory Controller Block Diagram

6.2.1 HT132 CPU/Memory Controller – Pinouts

The pin connections for the *HT132 CPU/Memory Controller* are shown in Figure 6-2. The pins are numbered sequentially in a counter-clockwise direction from the index mark as viewed from the botton of the chip.

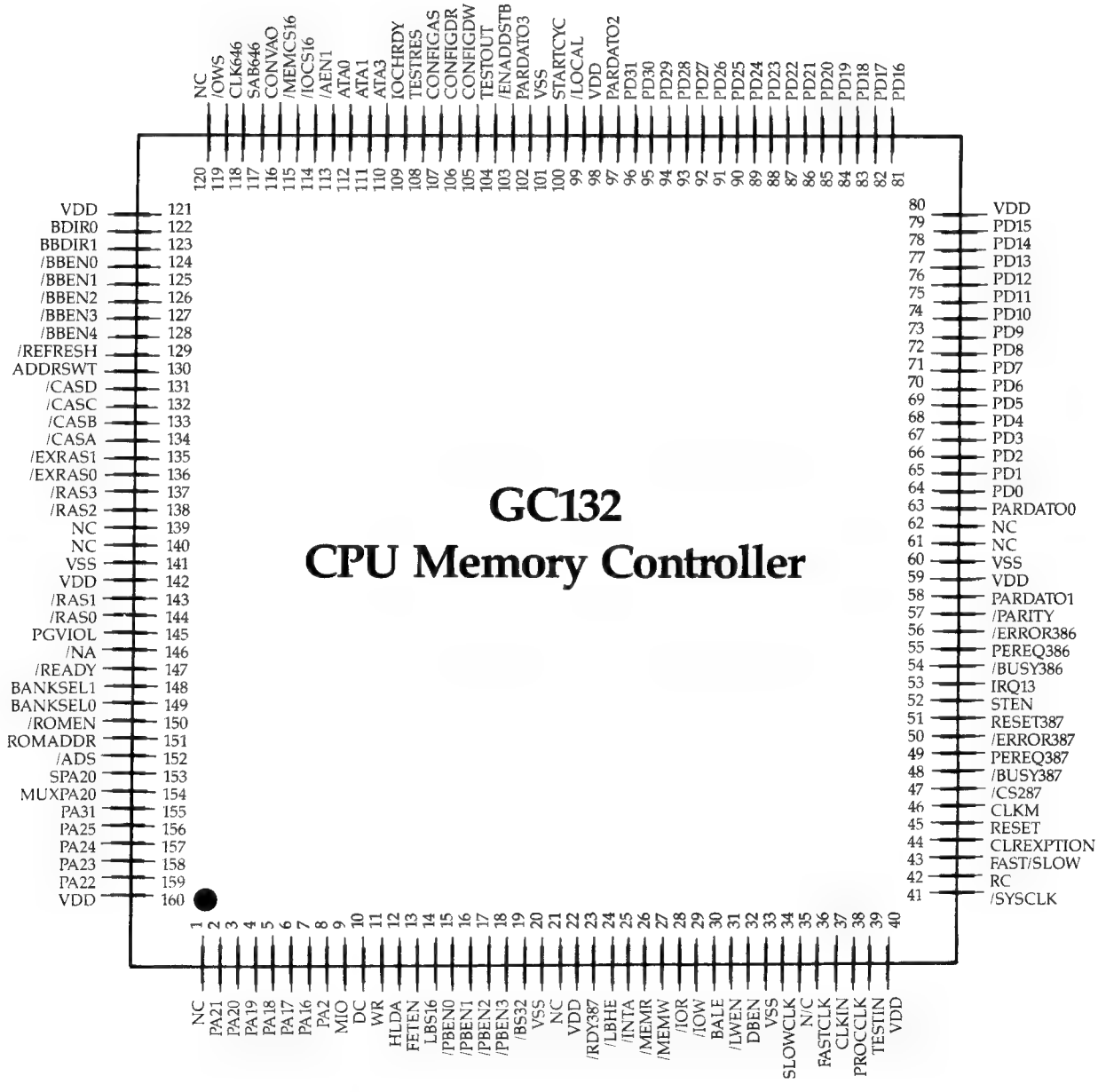


Figure 6-2. HT132 CPU/Memory Controller Pinouts

6.2.2 HT132 CPU/Memory Controller Pin Descriptions

This section describes the pins of the *HT132 CPU/Memory Controller.* The pin idenification numbers correspond with those shown in *Figure 6-2 - Pinouts, HT132 CPU/Memory Controller* on Page 17.

Pin Symbol	Pin Number	Pin Type	Description
ADDRSWT	130	O	**Address Select:** Selects either row or column addresses.
/ADS	152	I	**Address Status:** This signal marks the start of each memory or I/O cycle. Indicates that a valid bus cycle definition and an address are available. /ADS is active LOW on the same clock pulse as the driven addresses. /ADS is not driven during a bus HOLD.
/AEN1	113	I	**Address Enable:** Active during DMA but not during a MASTER access. Indicates 8 bit DMA access.
ATA0, ATA1, ATA3	112, 111, 110	I	**AT Backplane Address** A0, A1, A3.
BALE	30	O	**Buffered Address Latch Enable:** When HIGH the addresses are transparent between the processor side to the backplane side. On the falling edge the addresses are latched and held until another BALE.
BANKSEL0 BANKSEL1	149, 148	O	**Demultiplexer Select** specifies which bank is to receive the CAS strobes.
/BBEN0 to /BBEN4	124, 128	O	**Bus Bridge Data Enable:** BBEN0-3 enable the data buffers between the processor and the backplane. One signal per byte. BBEN4 enables the buffer between the upper and lower bytes on the 16 bit backplane bus.

Pin Symbol	Pin Number	Pin Type	Description
BBDIR0 BBDIR1	122 123	O	**Bus Bridge Direction Indicators:** BBDIR0 turns the direction of the buffer between ATD0-7 and ATD8-15. When HIGH the buffer will drive from lower 8 bits to upper 8 bits. The BBDIR1 signal indicates the data flow from processor to/from backplane. When HIGH the data will flow from the processor to the backplane, when LOW the flow is in the opposite direction.
/BS32	19	I	**Bus Size 32-Bits:** When LOW, this signal indicates that the current cycle is intended for local 32-bit access: LBS16 is inactive and /BBENs are in the OFF condition. (*See also* FETEN)
/BUSY386	54	O	**Busy 386:** Connects to the 'BUSY' line of the 80386 Microprocessor.
/BUSY387	48	I	**Busy 387** is connected to the 'BUSY' line of the 80387 Coprocessor.
/CASA to /CASD	134 to 131	O	**Column Address Timing Strobe** for the 4 bytes. These signals must be steered to the correct bank using BANKSEL or external logic for Banks 4 and 5.
CLK646	118	O	**Clock** the LS646 megafunction in the *HT133 Interface:* The rising edge latches the data presented on the lower 8 bits of the backplane. This is used on an 8 to 16 bit read conversion cycle.
CLKIN	37	I	**Clock:** This clock drives the entire chip on the rising edge. This clock is the same as used by the 80386 Microprocessor.
CLKM	46	O	**Clocking Mode:** When LOW it selects the asynchronous clocking mode of the 80387: when HIGH the synchronous mode. (See 'INDEX 01h' on Page 46).

Pin Symbol	Pin Number	Pin Type	Description
CLREXPTION	44	O	**Clear Exception:** Connects to the RESET of the 80386 Microprocessor. This is a synchronous reset.
CONFIGAS	107	I	**Configuration Register Address Strobe:** The configuration register index is strobed in on the falling edge of this signal from the data bus LD0-7. Results from an IOW to Address 24h.
CONFIGDR	106	I	**Configuration Register Data Read:** Data is read from the configuration register addresses by the value written in by the CONFIGAS pulse. This results from an IOR from Address 28h.
CONFIGDW	105	I	**Configuration Register Data Write:** Data is written on the falling edge into the register addressed by the Index latched by CONFIGAS.
CONVAO	116	O	**Conversion Address 0:** During an 8- to 16-bit conversion cycle, the 'address 0' line must be forced to a '1' during the second half. This signal tells the *HT133* when to force A0 to A1 on the backplane.
/CS287	47	I	**Chip Select 287 (Coprocessor).** When LOW the processor is addressing an I/O location between F0h-FFh.
DBEN	32	O	**Data Bus Enable:** When LOW, the local bus is expecting data from the *HT133*, when HIGH the *HT133* should not put data on the local bus.
DC	10	I	**Data or Control:** Status line from the 80386 Microprocessor.
/ENADDSTB	103	O	**Enable Address Strobe:** When LOW the *HT131* disables any access to the Real Time Clock. This signal is LOW from reset to the first processor access.

Pin Symbol	Pin Number	Pin Type	Description
/ERROR386	56		**Error (Coprocessor):** Signals the microprocessor that an error has occurred in the coprocessor.
/ERROR387	50	I	**Error** line from the 80387 Coprocessor.
/EXRAS0, /EXRAS1	136, 135	O	**Row Address Strobes** for Banks 4 and 5.
FASTCLK	36	I	**Main Oscillator Clock:** Between 32MHz and 50MHz.
FAST/SLOW	43	I	**Speed Switch:** When HIGH the output of the clock synchronization circuit (PROCCLK) is a buffered version of the FASTCLK input. When LOW the PROCCLK signal is a buffered version of the SLOWCLK input. This signal comes from the 8042.
FETEN	13	I	**Feature Enable:** When HIGH the features associated with pins /BS32, STARTCYL, and /LOCAL are enabled.
HLDA	12	I	**Hold Acknowledge:** When HIGH the processor has relinquished the address, data and status bus, when LOW the 80386 is the bus master.
/INTA	25	O	**Interrupt Acknowledge:** Indicates that the interrupt vector should be read into the processor.
IOCHRDY	109	I	**I/O Channel Ready:** A signal from the AT backplane requesting additional command active time. When LOW the chip will add any number of wait states until the signal is released.
/IOCS16	114	I	**I/O Chip Select is 16 Bits:** When asserted by a 16 bit device on the AT backplane, the chip will not perform a 8 to 16 bit conversion cycle. If it is inactive the *HT132* will assume the I/O cycle is to an 8 bit device. (Note: This signal refers to the device responding to the cycle, not the cycle itself.)

Pin Symbol	Pin Number	Pin Type	Description
/IOR	28	I/O	**I/O Read:** Normally an output, see the output pin definitions, but during DMA or MASTER mode, it becomes in input driven by the DMA controller.
/IOW	29	I/O	**I/O Write:** Normally an output, (See the *Output Pin Definitions)*, but during DMA or MASTER mode, it becomes an input driven by the DMA controller.
IRQ13	53	O	**Interrupt Request 13:** When HIGH the coprocessor has detected an exception and has raised an interrupt.
/LBHE	24	I	**Latched Bus HIGH Enable In:** Indicates when the upper 8 data bits of the 16 bit backplane is active.
LBS16	14	O	**Latched Bus Size 16:** When active the *HT132* is signalling the processor that the current cycle is inappropriate for 16 bit backplane operations, and the processor will adjust its cycle or issue another.
/LOCAL	99	O	**Local Bus Access:** When LOW indicates that the current cycle is used for local bus access and not for the backplane. *(See also* FETEN.)
/LWEN	31	O	**Latched Write Enable:** When active the current cycle is a write. A latched version of (WR). Used to indicate a WRITE operation to the DRAMs.
/MEMCS16	115	I	**Memory Chip Select is 16 Bits:** Indicates that the current cycle is addressing a 16 bit memory device and the *HT132 Controller* will not perform an 8 to 16 bit conversion cycle.
/MEMR	26	I/O	**Memory Read:** Normally an output, but during a DMA or MASTER mode cycle, it becomes an input and is used for determining the direction and duration of the *HT133 Bus Bridge* buffers.

Pin Symbol	Pin Number	Pin Type	Description
/MEMW	27	I/O	**Memory Write:** Normally an output, but during a DMA or MASTER mode cycle, it becomes an input and is used for determining the direction and duration of the *HT133 Bus Bridge* buffers.
MIO	9	I	**Memory or I/O status line** derived from the 80386 MIO.
MUXPA20	154	I	**Multiplex Processor Address 20:** When LOW the output SPA20 follows PA20 exactly. When HIGH SPA20 is forced LOW.
/NA	146	O	**Next Address:** When active the *HT132* is requesting that the next cycles address and ADS be issued.
/OWS	119	I	**Zero Wait State**
PA2	8	I	**Processor Address Line 2:** Used to determine which bank of DRAM will be interleaved next.
PA15 to PA25	7-2, 21, 159-156	I	**Processor Address Lines 15 Through 25:** Used for memory map control.
PA31	155	I	**Processor Address Line 31:** Used for coprocessor interface and the restart vector.
PARDATO0 to PARDATO3	63, 58, 97, 102	I/O	**Parity Data Out 0 Through 3:** During a memory read these pins are inputs which contain the parity data bit from the DRAM. These will be checke against a calculated version based on the LD0-31 lines. If there is an error the /PARITY signal will go active in the next bus cycle. During a memory write, these lines are outputs containing the calculated parity for each byte.
/PARITY	57	O	**PARITY Check:** When active at the end of a memory read cycle it indicates a parity error on the DRAM.

Pin Symbol	Pin Number	Pin Type	Description
/PBEN0 to /PBEN3	15-18	I	**Processor Byte Enable:** Indicates which of the four processor data bytes has valid data.
PD0 to PD7	64-71	I/O	**Processor or DRAM Data Lines:** Lower 8 bits are actually bi-directional. They are inputs during a configuration register WRITE or a memory READ for PARITY generation.
PD8 to PD31	72-79, 81-96	I	**Processor or DRAM Data Lines:** Always inputs, used for calculating parity during memory reads.
PEREQ386	55	O	**Processor Extension Request:** Connected to the 'PEREQ' line of the 80386 Microprocessor.
PEREQ387	49	I	**Processor Extension Request:** Connected to the 'PEREQ' line of the 80387 Coprocessor.
PGVIOL	145	I	**Page Violation:** During a memory operation the *HT133* will constantly compare the current DRAM page strobed in by the RAS signal with the current page presented by the processor for the next cycle. If the two pages are different this signal will go active.
PROCCLK	38	O	**Processor Clock:** The main clock that drives the 80386 (and 80387 and 80385 if fitted). This signal can be buffered or even inverted since the HT132 Controller does not use this clock: CLKIN is used to drive the internal state machines.
/RAS0 to /RAS3	144, 143 137, 138	O	**Row Address Strobe:** For the DRAMs.
RC	42	I	**Processor Reset:** When active the 8742 keyboard controller is requesting that the CPU be reset but NOT the system.

Pin Symbol	Pin Number	Pin Type	Description
/RDY387	23	I	**Ready** (from the 80387): When LOW the 80387 Coprocessor is terminating its cycle.
/READY	147	O	**Ready** (to the 80386): Terminates the cycle.
/REFRESH	129	I	**REFRESH:** Indicates that the current DMA cycle is a REFRESH operation and the *HT132* will not produce a CAS signal, just a RAS.
RESET	45	I	**RESET (System):** When active the CPU and the entire system will be reset.
RESET387	51	O	**RESET (80387):** A synchronous reset to the 80387 Coprocessor.
ROMADDR	151	O	**HIGH ROM Address:** Connects to A16 on a 27512 or VPP on a 27256. When the configuration bit is set for 27512 usage, this line will follow a latched version of PA16, when set for a EPROM 27256, it will remain at VDD.
/ROMEN	150	O	**EPROM Enable:** Connects to the OE of the EPROM. It indicates when the device should drive the data bus.
SAB646	117	O	**Select Latched or Transparent Data:** When LOW the *HT133* will (on a READ) allow un-inhibited data flow from the backplane to the processor local bus. When HIGH the *HT133* will present the data latched by CLK646 to the lower byte on the local data bus. This is used during an 8 to 16 bit read conversion cycle.
SLOWCLK	34	I	**SLOW System Clock** (Frequency = 14.318MHz): Used for the system clock during slow speed the FAST/SLOW signal is LOW.
SPA20	153	I/O	**Switched Processor Address 20:** Normally this signal is an output that follows PA20 (except when MUXPA20 is HIGH), but during a DMA or MASTER mode, SPA20 is the Address line 20 input.

Pin Symbol	Pin Number	Pin Type	Description
STARTCYC	100	O	**Start a DRAM Cycle:** Useful when implementing a memory sub-system external to the *HT132,* this signal indicates the start of a DRAM cycle. Defined as RAS and /CAS, this signal helps with the problem of knowing when to initiate a /CAS precharge during a page mode cycle. (*See also* FETEN.)
STEN	52	O	Connects to the STEN line of the 80387 Coprocessor.
/SYSCLK	41	O	**System Clock:** Main clock for the *HT131,* equivalent to CLKIN divided by 2.
TESTIN	39	I	**Test Mode Enable:** Used for fault coverage in the fabrication process. Not user applicable.
TESTOUT	104	O	Factory test pin. Normally not connected.
TESTRES	108	I	**TEST Reset:** Used for fault coverage in the fabrication process. Not user applicable.
WR	11		**Write-Read:** Status line from the 80386.
VDD	22, 40, 59, 80, 98, 121, 142, 160	**5 volts**	
VSS	20, 33, 60, 101, 141	**Ground**	

6.3 PROGRAMMING THE CONFIGURATION REGISTERS

This Section explains how the configuration-bit registers can be used to optimise the EPROMs of an 80386-based personal computer system. In this use, the *HT132 CPU/Memory Controller's* functions are particularly important.

The *HT132 Controller* operates in the 32-bit mode: a/ to control the general bus timing relationships for RAM, ROM, and I/O; b/ to control the size of RAM and ROM blocks; and c/ to adjust the system when using an 80287 or 80387 Coprocessor.

The configuration registers of the *HT132 Controller* are partitioned according to their duties. One register set operates system timing, another is concerned with system hardware, and a third set configures the memory map.

- Memory map reconfiguration
- Faster operation through 'shadowing' – plus, the ability to establish either 32K or 64K Video BIOS space
- Startup configuration
- Multiple banks of DRAM
- Reclaim RAM with REMAPPING

BIOS Patches Used to Implement Required Defaults

A convenient method by which the defaults can be established, for the 80386 Microprocessor and the computer system, involves the use of a BIOS patch.

6.3.1 Reconfiguring the Memory Map

The memory map of the *HT132 CPU/Memory Controller* is compatible with the AT specification. And, in addition, the controller has features that allow greater memory capacity, improved performance, and the ability to use operating systems other than DOS.

Compatibility with the AT-Design

The AT design maintains upward compatibility with the earlier XT design. In consequence, the memory map of an XT system can be described as a sub-set of an AT memory map. Because the XT design is limited to a memory space of one megabyte only that amount, the lower 1Mb, of the AT's memory map must satisfy the needs of compatibility. The remainder (a further 15Mb) is called 'backplane' memory. A small area of this upper memory is reserved for a mirror image of BIOS – needed for the RESTART vector, is located at the top of the four gigabytes of 80386 memory.

EPROM Memory Map

The needs of compatibility require the EPROM BIOS, or 'Lower BIOS', at F0000h through FFFFFh and, for system start, 'Upper BIOS' is located at FFFF0000h (*See Figure* 6-3). But modifications can be made to the memory map - as explained in the following pages - using these tools:

- MBEN is a device used to regulate the memory space associated with a copy of BIOS (called 'Middle BIOS'). MBEN, when disabled, frees this memory space when operating systems (non-DOS) do not require BIOS in this memory region. MBEN acts within an area of memory described as 'Window 3'.

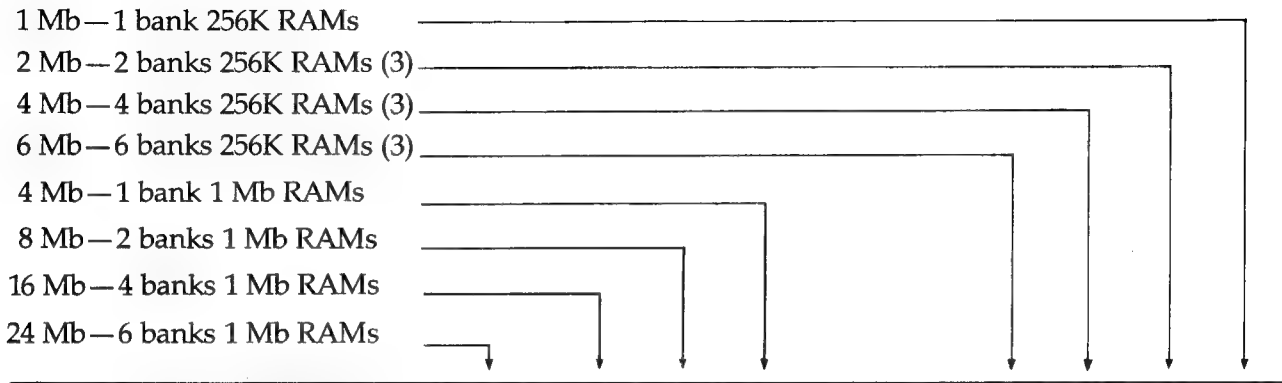
- LBSHADOW is a device used to implement a 32-bit (rather than a 16-bit) version of BIOS called 'Lower BIOS' located within an area of memory described as 'Window 2'.

- MBSHADOW is a device used to implement a 32-bit version of BIOS called 'Middle BIOS' located in memory at 'Window 3'. MBSHADOW operates when the MBEN device is enabled.

- VBSHADOW is a device used to implement a 32-bit version of Video BIOS: a replacement of the 16-bit version in the memory region called 'Window 1'.

- VBEN is a device used to regulate the shadowing of Video BIOS. When enabled the system takes the configuration established by VBSHADOW.

Memory Map



Absolute Addresses	24	16	8	4	18	10	6	4	2	1
0h—0FFFFh	32-Bit on-board RAM									
A0000h—BFFFFh	AT-compatible RAM									
C0000h—CFFFFh	Video BIOS (2)									
D0000h—DFFFFh	AT-compatible RAM									
E0000h—EFFFFh	Lower BIOS (2)									
F0000h—FFFFFh	Lower BIOS (2)									
100000h—1FFFFFh	32-Bit on-board RAM									
200000h—3FFFFFh										
400000h—5FFFFFh							OBR			
600000h—7FFFFFh										
800000h—9FFFFFh										
A00000h—FDFFFFh			AT-compatible RAM							
FE0000h—FEFFFFh										
FF0000h—FFFFFFh										
1000000h—11FFFFFh			Not used							
1200000h—17FFFFFh										
1800000h—FFFDFFFFh										
FFFE0000h—FFFEFFFFh	Upper BIOS (2)									
FFFF0000h—FFFFFFFFh	EPROM									

Notes: (1) Banks 5 and 6 operate exactly as the other banks; but, they are configured by a separate register.
(2) Memory type in these locations is dependent upon the configuration registers and the EPROM type used.
(3) Interleaving is performed on A2 when more than one bank of memory is used.
(4) OBR = On-board 32-Bit RAM.

Figure 6-3. HT132 Memory Controller, Memory Map

A Definition of Offboard Memory

Offboard (or backplane) memory is that memory space where EPROM or DRAM is not located. Conversely, if it isn't EPROM or DRAM space then it is backplane memory space. Backplane space includes all of the vast area above DRAM to the 4Gb top. Backplane is assumed to be either eight or sixteen bits in width as determined by the status of the /MEMCS16 signal.

6.3.2 MBEN and Non-DOS Operation

The *ATLAS Chip Set* has programmable configuration bits (as described later in Chapter 8 - *The Configuration Registers*). Of these, MBEN (meaning, 'Middle BIOS enable') is used to alter the EPROM memory space when applications are run under operating systems other than DOS.

MBEN's purpose is to enable and disable the EPROM BIOS at memory space FF0000h. This, as shown in Figure 61, removes Middle BIOS from memory. It's a useful feature. When UNIX® is used as the operating system and with 24Mb of DRAM in use, middle BIOS is not needed. When removed, a contiguous DRAM space is made available. Without the MBEN feature, an inconvenient hole at FF0000h would otherwise exist.

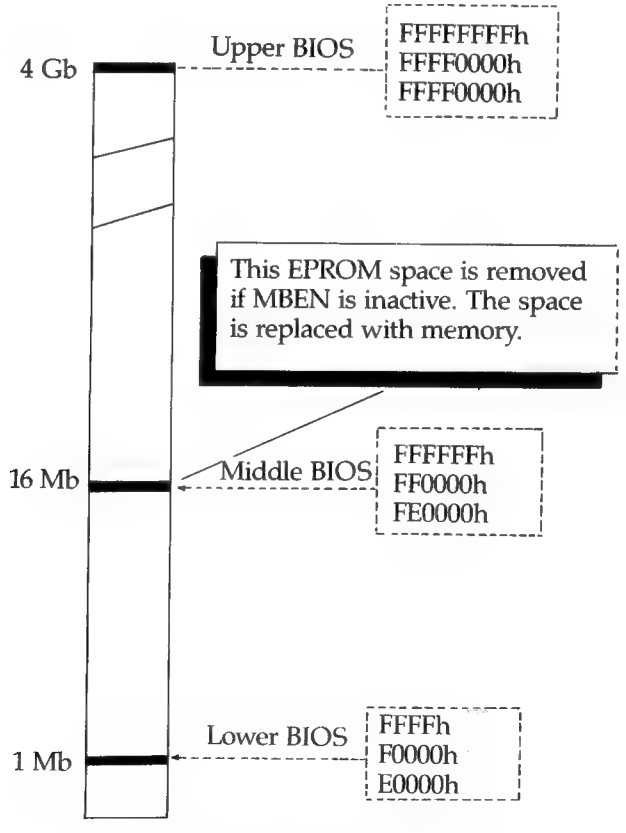


Figure 6-4. EPROM Memory Map

How to Use MBEN to Remove Middle BIOS

MBEN is signalled by INDEX01h (See Chapter 8 *'General setup bits'*) where Bit 6 is set to '0' to disable and '1' to enable MBEN.

6.3.3 Programmable Configuration Bits Allow RAM 'Shadowing'

The *ATLAS Chip Set* has a built-in 'shadowing' feature that allows the copying of the BIOS (EP) ROMs to RAM for faster execution of ROM based code.

When a shadowed BIOS is accessed by the 80386 Microprocessor, the data is fetched from high speed 32-bit RAM instead of the slower 16-bit ROM on the motherboard; or even slower yet, from 8-bit access through the expansion bus.

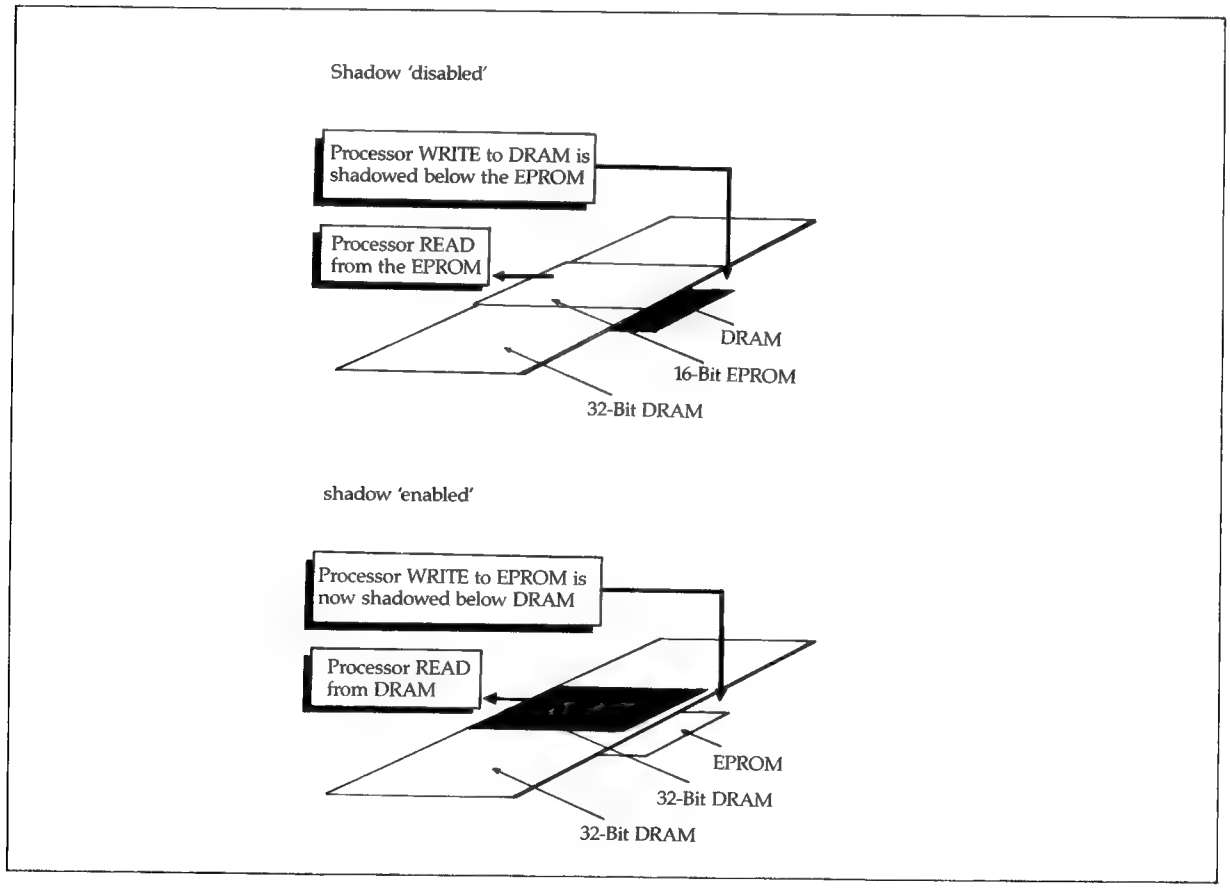


Figure 6-5. RAM Shadowing

How the RAM 'Shadow' Feature Works

The shadow RAM feature initially routes READ operations to the physical ROM and WRITE operations to the shadow RAM. At system start, a routine in the system BIOS makes a copy of the ROM modules to RAM by copying the BIOS back to itself: a 32-bit copy replaces the 16-bit version. The *HT132 CPU/Memory Controller* arranges the READ and WRITE operations in such a way that the ROM contents are duplicated in shadow RAM.

When the cloning operation is done, the bootstrap routines switch the *HT132 Controller* into shadow-mode. The shadow memory windows are used in this manner:

- During READ operations, access is given to the shadow RAM.
- During WRITE operations, the *HT131 Controller* gives access to the ROMs; but, /ROMEN (the EPROM Enable signal) remains inactive – a technique to protect the shadow RAM. All WRITE data operations are dumped into the proverbial bit bucket: it's impossible to write to ROM.

6.3.4 Four Memory Windows

The *ATLAS Chip Set* accesses the system ROMs through four memory 'windows' and, as noted on the next page, Window 1 can be split to accommodate either 32K or 64K Video BIOS.

Two variants of the four-window definition are used: one for each type of ROM chip used in the system. The EPROMs canbe either, Type 27256 (Table 6-1) or Type 27512 (Table 6-2).

When EPROM Type 27512 is used Windows 2, 3 and 4 are larger. *See Note**

Window	Range	Use
1	C0000h-CFFFFh (As noted in the next section, this space can be further split into C0000h – C7FFF7 C8000h – CFFFFh)	Video BIOS
2	F0000h – FFFFFh	Lower BIOS
3	FF0000h – FFFFFFh	Middle BIOS
4	FFFF0000h – FFFFFFFFh	Upper BIOS

Table 6-1. Memory Windows, EPROM Type 27256

Window	Range	Use
1	C0000h - CFFFFh (As noted in the next section, this space can be further split into C0000h - C7FFFh C8000h - CFFFFh)	Video BIOS
2	E0000h - FFFFFh	Lower BIOS
3	FE0000h - FFFFFFh	Middle BIOS
4	FFFE0000h - FFFFFFFFh	Upper BIOS

Table 6-2. Memory Windows, EPROM Type 27512

Note: The installed chip's type is signalled by the setting of INDEX01h 'General setup bits'. This, as noted in 'Chapter 8 - The Configuration Registers', Bit 2 is to be set to '0' when EPROM Type 27256 is used; and set to '1' with the 27512.

6.3.5 Video BIOS Space in Window I can be Split

32K Video BIOS Feature Releases Space for RAM or Backplane Memory

Useful in systems that need only 32K Video BIOS space, the *ATLAS Chip Set* allows the allocation of either 32K or 64K space (within Window 1) for Video BIOS. Released space can be used for RAM or backplane memory. Here's how it works.

INDEX0Fh (Bits 2 and 3) Adjust Video BIOS Space

When **64K Video** BIOS space is required INDEX0Fh (Bits 2 and 3) remain at their default setting of '0'.

For **32K Video** space allocation: Bit 3 is set to '1' and Bit 2 designates, by its condition, the region in which the system expects to find the 32K Video BIOS. Bit 2 is set to '0' when the 32K chunk resides in the region bounded by C0000h-C7FFFh. Bit 2 is set to '1' when the chunk resides in C8000h-CFFFFh.

Notes: 1. If Bit 3 if INDEX0Fh is set to '0' the condition of Bit 2 is ignored.
2. If Bit 3 = '1' *and* Bit 2 = '0' the Video BIOS must reside between C0000h-C7FFFh.
   If Bit 3 = '1' *and* Bit 2 = '1' the Video BIOS must reside between C8000h-CFFFFh.
3. With the 32K Video BIOS feature enabled, the unallocated 32K of memory space is available for RAM or backplane memory.

Video BIOS (Both 32K and 64K Versions) can be Shadowed

As discussed next, the Video BIOS (in either 32K or 64K size) can be shadowed.

6.4 RAM SHADOWING (WINDOWS 1 THROUGH 3)

The *ATLAS Chip Set* supports shadowing for Windows 1, 2 and 3. Access through Window 4 is always direct to the system BIOS ROMs.

Each window has its own special behaviour when shadowing.

6.4.1 Window 1 – Video BIOS Shadowing

The Video BIOS window is reserved for ROM modules fitted to video-adapter cards and similar devices.

By default (after startup) all READ and WRITE accesses to this window are directed to the 16-bit AT expansion bus.

The default mode for Window 1 accommodates unconventional usage of the video BIOS address range by network-adapter cards and other devices that put dual-ported RAM at this location. In the default mode, the cards function in the normal ('AT') manner.

VBEN Uses INDEX 01h, Bit 4

To use the Video BIOS memory window for the Video BIOS set INDEX01h Bit 4 to '1'. All WRITE operations are thus routed to RAM and all READ operations are routed to the expansion bus.

VBSHADOW Uses INDEX 01h, Bit 0

The Video BIOS can be copied to shadow RAM by writing it byte-for-byte back to itself: the 32-bit version replaces the 16-bit. When the cloning operation is complete, high speed access of video BIOS routines (in shadow RAM) is activated by setting Bit 0 of INDEX01h to '1'.

The physical memory used for shadowing the Video BIOS is located at C0000h - CFFFFh. (*See 'Video BIOS space in Window 1 can be split'*). The system must have enough installed RAM to populate this region of the memory map.

6.4.2 Window 2 – Lower BIOS

By default (after startup), the Window 2 memory space is a 'shadowed' copy of the Window 4 address space. Any READ operations cause access to the Window 4 space: WRITE operations are directed to shadow RAM.

LBSHADOW Uses INDEX 00h, Bit 6

In a manner similar to that of Video BIOS shadowing, the bootstrap routine must copy the Lower BIOS back to itself: the 32-bit version replaces the 16-bit. When cloning is complete the program can set Bit 6 of INDEX00h to '1' that activates the use of the 32-bit Lower BIOS access.

The physical memory used for shadowing the Lower System BIOS is located at F0000h FFFFFh for Type 27256 EPROMs. (Location E0000h-FFFFFh for Type 27512 EPROMs.) The system must have enough installed RAM to populate this region of the memory map.

6.4.3 Window 3 – Middle BIOS

In a manner similar to the Video BIOS shadowing, the bootstrap must copy the Middle BIOS back to itself.

MBSHADOW Uses INDEX 00h, Bit 7

When cloning is complete the program can set Bit 7 of INDEX00h to '1' to activate high speed Middle BIOS access.

The physical memory used for shadowing the Middle BIOS is located at FF0000h - FFFFFFh for Type 27256 EPROMs. (Location FE0000h - FFFFFFh for Type 27512 EPROMs.) The system must have enough installed RAM to populate this region of the memory map.

It should be noted that the cloning of Lower BIOS has no effect on Middle BIOS, nor does Middle effect Lower BIOS. If both BIOS systems are to be executed from shadow RAM, both Lower and Middle BIOS must be explicitly copied.

Caution: The combined use of both the shadow RAM feature and the REMAP feature (if Bit 5 of INDEX01h is set to '1') may cause the chip set to lock up. That, very effectively, crashes the host system.

6.4.4 Window 4 – Upper BIOS

Shadowing of Window 4 is not possible.

6.5 USE THE REMAP FEATURE TO SAVE UNUSED RAM SPACE

In the standard AT memory map configuration, address space from A0000h to FFFFFh is normally reserved for device and ROM usage. (*See Figure 6-3.*)

When more than 640K of memory is installed on an *ATLAS Chip Set*-based system, RAM that might otherwise be mapped into the device/ROM region is blanked out and is not accessible. For cost sensitive applications this represents an effective loss of up to 384K of expensive RAM memory.

This region of unused RAM can be reclaimed by activating the shadowing feature. With REMAP, up to 384K of memory becomes useful and is remapped into another section of the 80386 memory map. With REMAP, the user has the option of relocating this section of RAM memory to one of the address ranges shown below.

- Option 1 – Append to the first megabyte. (100000h to 15FFFFh.)
  Used only when 1Mb of memory is populated with 256K DRAMs (one bank installed).

- Option 2 – Append to the second megabyte. (200000h to 25FFFFh.)
  Used only when 2Mb of memory is populated with 256K DRAMs (two banks installed).

- Option 3 – Append to the fourth megabyte. (400000h to 45FFFFh.)
  Used only when 4Mb of memory is populated with 1Mb DRAMs (one bank installed).

The REMAP feature cannot be used with memory configurations other than those noted above.

Caution: The combined use of both the shadow RAM feature and the REMAP feature (if Bit 5 of INDEX01h is set to '1') may cause the chip set to lock up. That, very effectively, crashes the host system.

How to activate REMAP

The REMAP feature is activated when these conditions are true:

1. The Shadow RAM feature is turned OFF,
2. The amount of memory in the system has been configured, then
3. Bit 5 of the general setup register INDEX01h is set to '1', and
4. Bit 3 of DRAM configuration register INDEX10h is set to '1'.

Caution: If these three conditions are not true – and especially if the register bits 01h and 10h are set before memory has been configured – the chip set will be confused as to which REMAP option (1, 2, or 3) to use. This may result in erratic system operation.

More About REMAP

Once the REMAP feature is turned ON, 32-bit shadow RAM is not available and any user who attempts this may corrupt the memory map.

A feature associated with remapping modifies the earlier comment. The DRAM located from 640K (A0000h) to 1Mb (FFFFFh) is remapped to a different location when REMAP is turned ON. Thus, there will be no DRAM available to shadow; instead, shadow will be to the backplane RAM. By this process, it is possible to use the backplane RAM for shadowing and still also activate the REMAP feature.

6.6 MEMORY MAP OF THE DRAM SUBSYSTEM

The DRAM control system is made complex by the variety with which the INDEX registers (described later in *Chapter 8 - The Configuration Registers*) can alter configuration, and effect the address space of the DRAMs used in the *ATLAS Chip Set*. The chip set can accommodate 256K DRAMs or 1Mb DRAMs. From one to six banks of page/interleave DRAM can be configured. And, several options exist with respect to the use of address space.

A Summary of the Available DRAM Configurations

A summary of the available DRAM configurations is listed in Figure 6-6.

Total Amount of RAM	Total Usable DRAM	DRAM type for each bank						REMAP Available	LB SHADOW	VB SHADOW	MB SHADOW
		0	1	2	3	4	5				
1Mb	1Mb	256K	–	–	–	–	–	Yes	Yes	Yes	No
2Mb	2Mb	256K	256K	–	–	–	–	Yes	Yes	Yes	No
4Mb	3.64Mb	256K	256K	256K	256K	–	–	No	Yes	Yes	No
6Mb	5.64Mb	256K	256K	256K	256K	256K	256K	No	Yes	Yes	No
4Mb	4Mb	1Mb	–	–	–	–	–	Yes	Yes	Yes	No
8Mb	7.64Mb	1Mb	1Mb	–	–	–	–	No	Yes	Yes	No
16Mb	15.64Mb	1Mb	1Mb	1Mb	1Mb	–	–	No	Yes	Yes	Yes
24Mb	23.64Mb	1Mb	1Mb	1Mb	1Mb	1Mb	1Mb	No	Yes	Yes	Yes

Figure 6-6. Summary of Available DRAM Configurations

6.6.1 One Bank of RAM

This-the single bank of installed RAM-is a special case because it is the only situation in which interleaving does not occur. At least two banks are required for interleaving.

The memory map for the single and double banks of installed RAM is illustrate in Figure 6-7. For clarity, the RAM shadowing, REMAP, and the EMS 'hole' features (described later in this Chapter) are disabled.

With 256K DRAMs, the memory capacity is 1Mb; but, due to the definition of the AT memory map, only the first 640K is reachable. The rest is defined as backplane memory.

If nothing is done to change this situation, the DRAM residing from 640K to 1Mb is wasted. If 1Mb DRAMs are installed the memory capacity is 4Mb; but again, the 384K above 640K is wasted. (See the *REMAP* Section).

The *ATLAS Chip Set* has allotted, within it, two shadow regions between 640K and 1Mb. These are described in the previous Section as EPROM shadowing and Video shadowing.

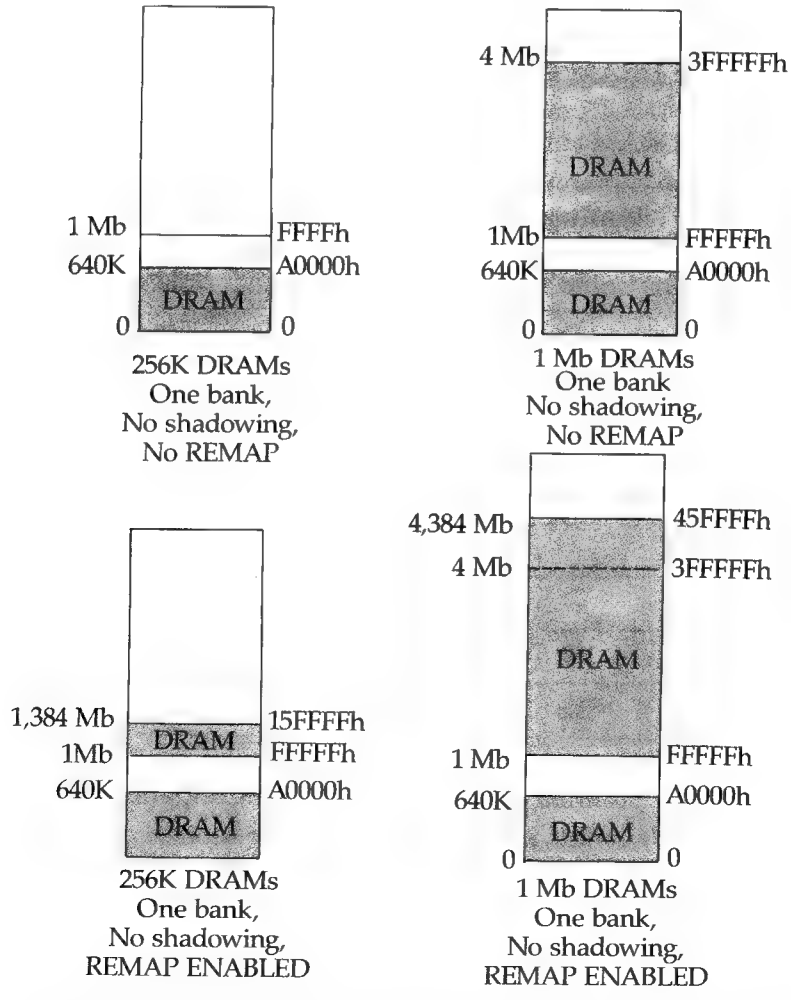


Figure 6-7. The Effects of REMAP with One Bank of RAM

6.6.2. Two Banks of DRAM

As soon as two banks of DRAM are recognized, the *ATLAS Chip Set* starts interleaving. Interleaving takes place on double-word boundaries. The memory map (Figure 6-8) shows two configurations - banks of 256K DRAMs and banks of 1Mb DRAMs.

Shadowing works, as before; but, REMAP does not. In order to allow the internal address decoder to be as simple as possible, the REMAP feature is implemented only on smaller configurations. For two banks of 1Mb DRAMs REMAP is not implemented. It is, however, implemented for two banks of 256K DRAMs.

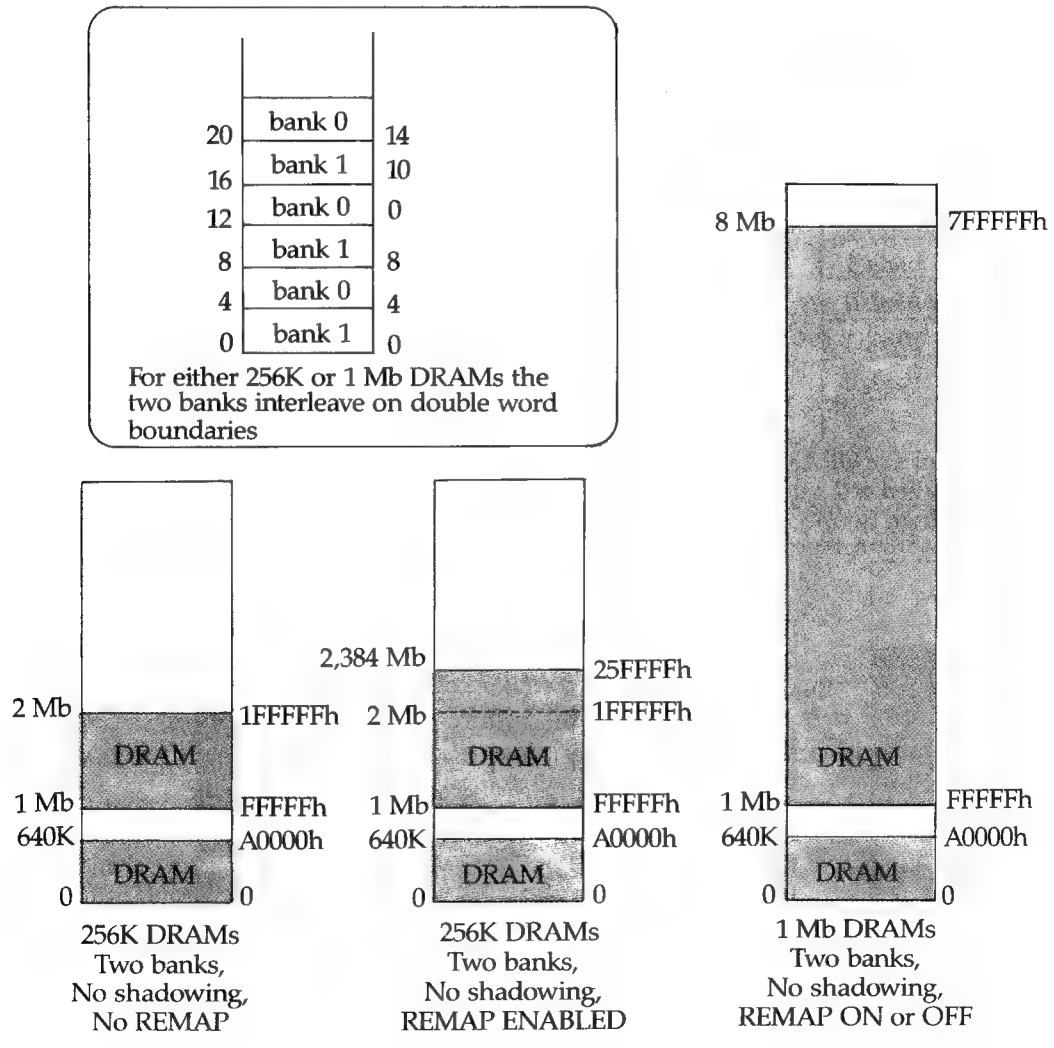


Figure 6-8. The Effects of REMAP with Two Banks of RAM

6.6.3 Four Banks of DRAM

As with the two banks of DRAM, four banks of DRAM will interleave but this is not, strictly speaking, four-way interleaving. As shown in Figure 6-9, if the processor is accessing Location 0, the consecutive reads are: BANK0, BANK1, BANK0, BANK1, BANK0, and so on.

This continues until (at a much higher address) the chip set switches to BANKS2 and 3. The interleaving then cycles in this manner: BANK2, BANK3, BANK2, BANK3, and so on.

The change (froM BANK0/BANK1 to BANK2/BANK3 interleaving) takes place at 2Mb for 256K RAMs and 8Mb for 1Mb RAMs.

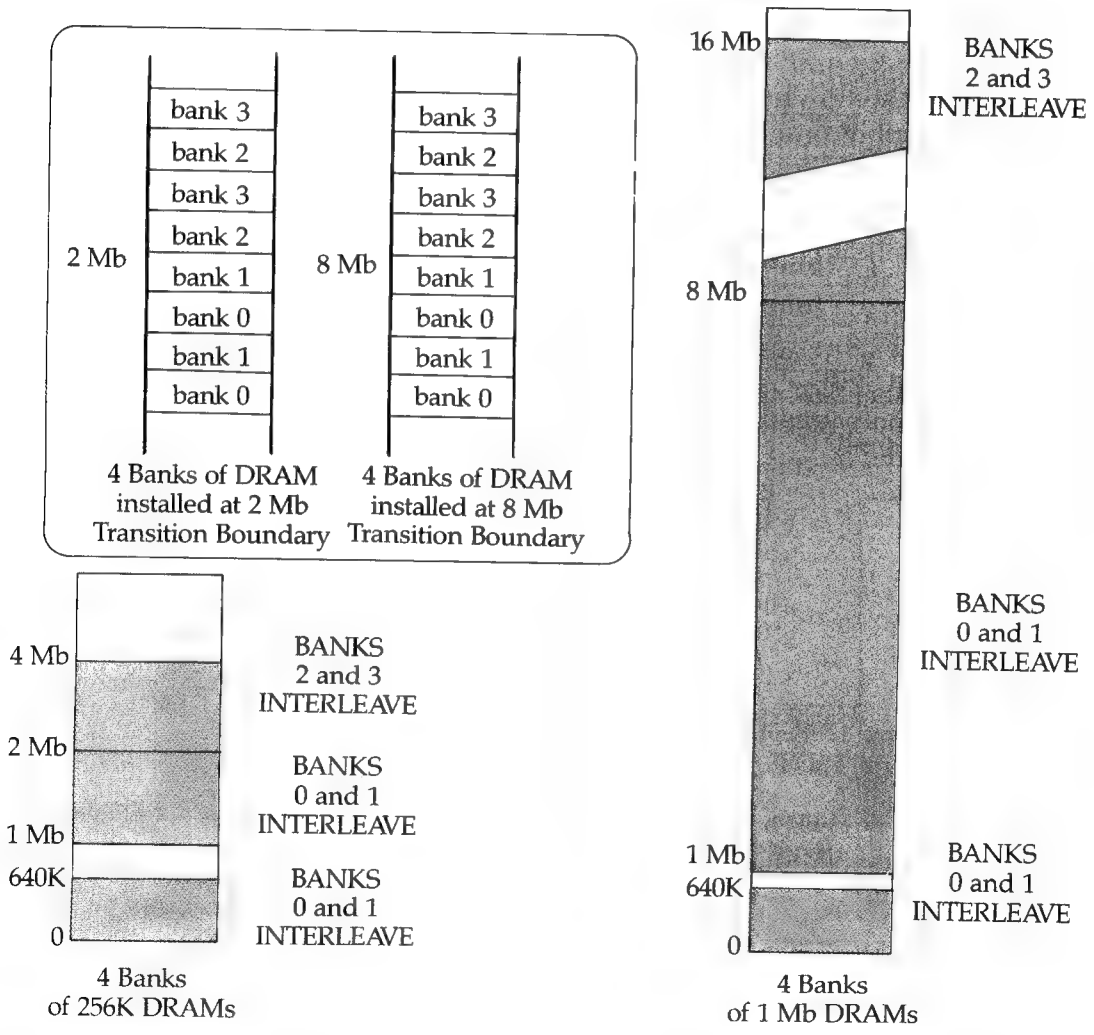


Figure 6-9. The Effects of REMAP with Four Banks of RAM

True 'four-way' interleaving requires the use of either four or eight banks

Incidentally, an example of 'true' four-way interleaving would follow the sequence: BANK0, BANK1, BANK2, BANK3, BANK0, BANK1, BANK2, BANK3, and so on. But, for this to work properly, the user's system must be fitted with an even multiples of four banks (either, 4 banks or 8 banks).

The user couldn't use this interleaving method with (for example) five banks of installed DRAMs. The modified four-way interleaving, on the other hand, which requires the use of paierd DRAMs is less restrictive on the user's configuration.

6.6.4 Six Banks of DRAM

When the last two banks are added, DRAM is treated in a different manner. The fifth and sixth banks have their own ENABLE configuration bits (INDEX00h, Bit 4) and their own set of timing configuration regsisters (INDEX05h). Typically, no machine has more than four banks of DRAM on the main memory board (due to the expense): above this point, in design, plug-in memory boards are used. The plug-in boards (typically) have buffered DATA, ADDRESS, and RAS/CAS signals which would necessarily have timing that differs from those of the on-board DRAM; hence, a new set of timing configuration registers are needed.

Once the banks are enabled, they must be populated with the same DRAMs as Banks 2 and 3. This means that Banks 0, 1, 2, and 3 must be populated before Banks 4 and 5 are turned ON.

6.7 EMS HOLE

The *ATLAS Chip Set* can be configured to accommodate a 64K 'hole', in the memory map, below 640K. This feature enables the use of EMS memory cards that need a 64K spot to position their memory (within the range 256K to 768K).

The 64K hole appears, to the system, as offboard RAM.

INDEX03h, in the *HT132 Controller,* configures this feature. The startup default places the 64K hole at A0000h. Figure 6-10 shows a sample memory map with the 'hole' placed at 40000h.

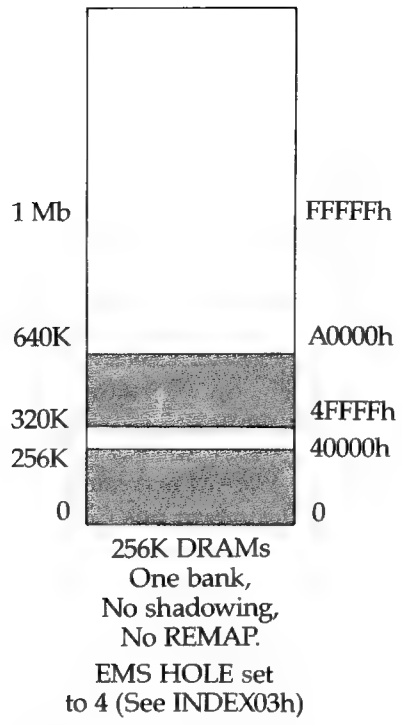


Figure 6-10. The EMS 'Hole'

6.8 CONNECTING MULTIPLE BANKS OF DRAM TO THE HTK131 CHIP SET

Up to Four Banks

The recommended method by which up to four banks of DRAM can be connected is shown in Figure 6-11 [Reference Application schematics 386APP-1].

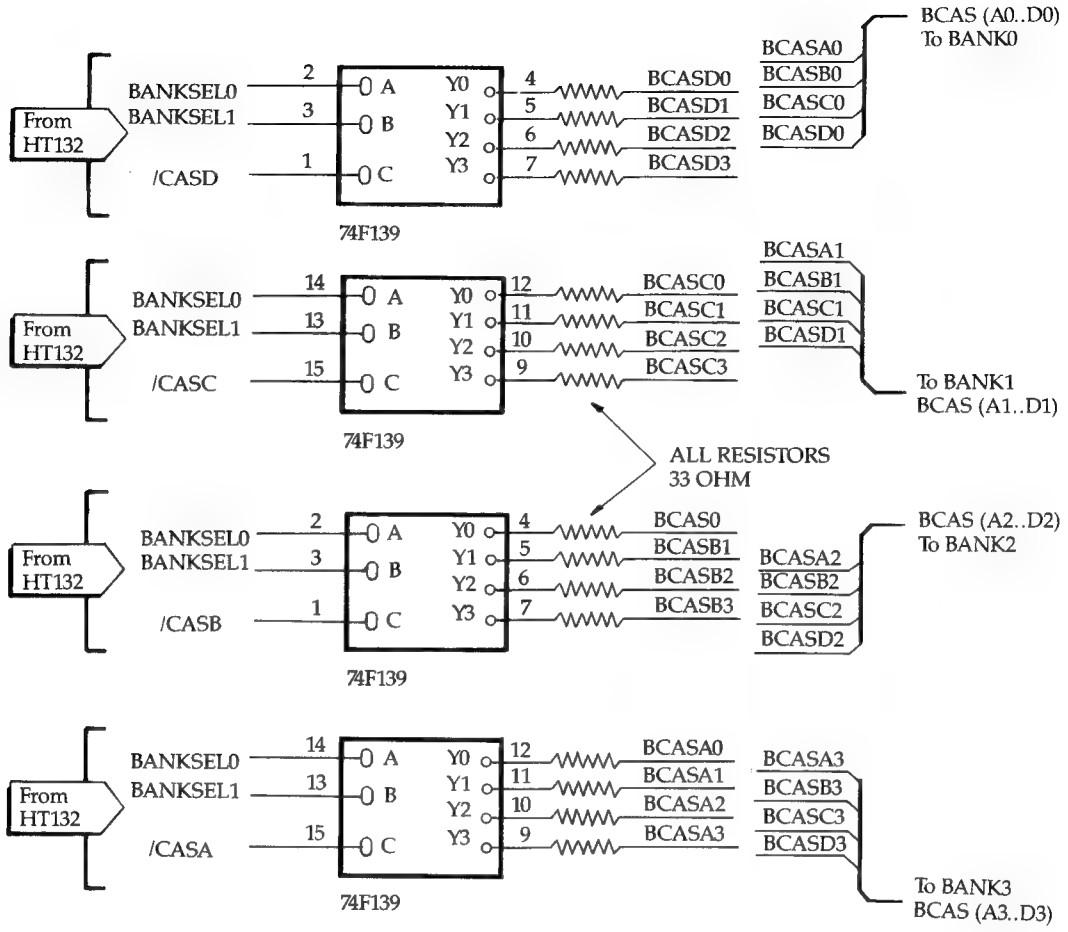


Figure 6-11. Connecting Four Banks of RAM

Six Banks

Since only two BANKSEL signals are available (and when six banks of DRAM are installed), Banks 4 and 5 must be selected in a manner different to that used for Banks 0 through 3.

For Banks 4 and 5, the recommended system makes use of the /EXRAS0 and /EXRAS1 signals (when the upper banks are selected). This is shown in Figure 6-12 (Reference Application schematic 386APP2).

In the drawing 386APP2, the NAND gate is required to ensure that only one bank can be selected at one time.

The individual /RAS lines (/RAS0.../RAS3 and /EXRAS0, /EXRAS1) are buffered by the 74F244 package for application directly to the corresponding bank. (See *Drawing 386APP5, Figure 6-13*) shows the recommended buffering and bank assignments.

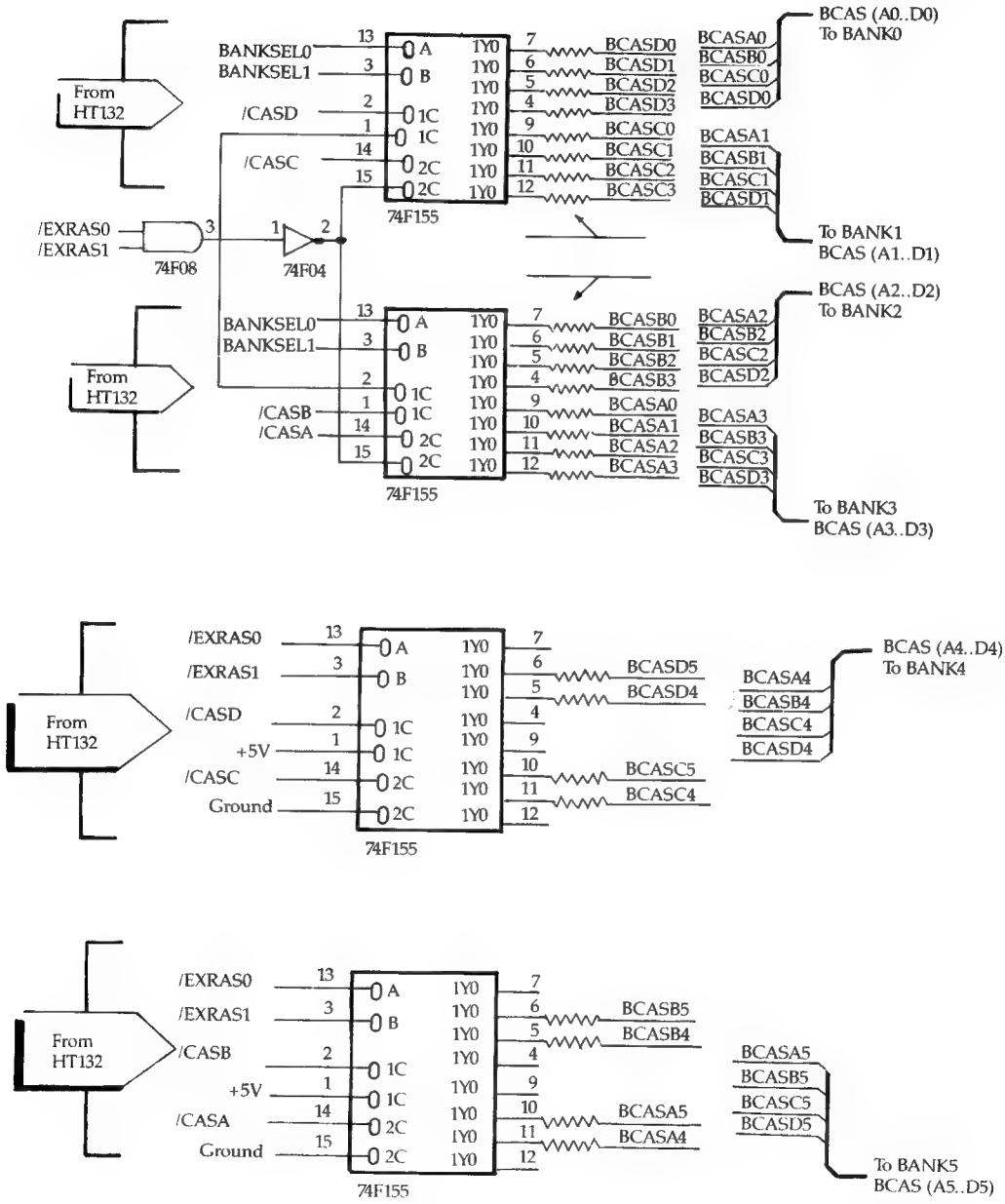


Figure 6-12. Connecting Six Banks of RAM

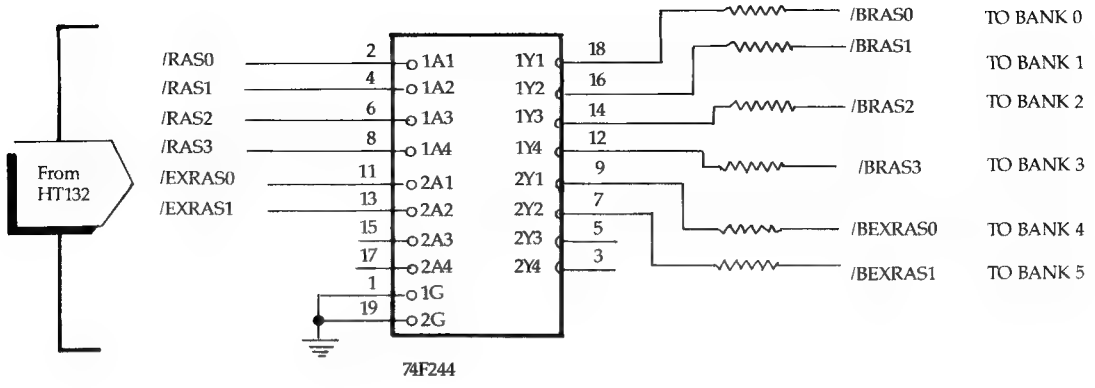


Figure 6-13. Connecting RAS Signals to the DRAMs

6.9 DRAM REFRESH

All DRAM require each memory cell to be refreshed at least once every four ms. To meet this requirement a system wide refresh cycle occurs every 15us. The system board conducts the refresh cycle to both ISA bus memory and 32-bit memory simultaneously. During the refresh cycle the CPU can still access cache.

An ISA bus secondary requesting agent (SRA) must initiate refresh cycle at appropriate intervals if it has control of the ISA bus for greater than 15us. The system board executed the refresh cycle, and then returns control to the SRA.

7

GC133 BUS BRIDGE INTERFACE

7.1 INTRODUCTION

This chapter provides an overview of the GC133 Bus Bridge Interface.

7.2 SEPARATION OF 32-BIT AND 16-BIT 'WORLDS'

For system implementation several buses are supported by the GCK131 Chip Set. Of these, the 32-bit processor address (PA) and data (PD) bus and the 16-bit address (ADA) and data (ATD) bus are particularly important to the system designer.

Figure 7-1 shows the functional block diagram of HT133 Bus Bridge Interface chip.

The PA and PD Bus

The PA and PD bus is high speed address and data bus that interfaces with the 80286 Microprocessor and the 80287 or 80387 numerical coprocessor. This bus also provides the local information path between all three chips of the GCK131 Chip Set. The address and the data paths of this bus are 32-bit wide as required to handle the full range of address and data values. In an AT system, I/O devices should not be directly connected to this bus:it is intended, solely, as a high speed interface.

The ATA and ATD Bus

The ATA and ATD bus provides the address and data requirements of the XT/AT expansion bus. This bus, a local to the GC131 Peripheral Controller, the GC133 Bus Bridge Interface, and the AT expansion bus, has a data width of 16 bits and the 24 bits of addressing that is required for AT standards.

The upper address bits required for the AT expansion bus are supplied by buffering the PA17 to PA23 lines of the PA bus. These, with ATA0 to ATA19, provide the necessary addresses for proper connection to the AT expansion bus.

The ATA and ATD bus, which generally operates at a slower speed than the PA and PD bus, allows the connection of all types of peripheral devices to the GCK131 supported AT system. To transfer data between the high-speed PD bus and the slower ATD bus, the GC133 Bus Bridge Interface is used at appropriate times.

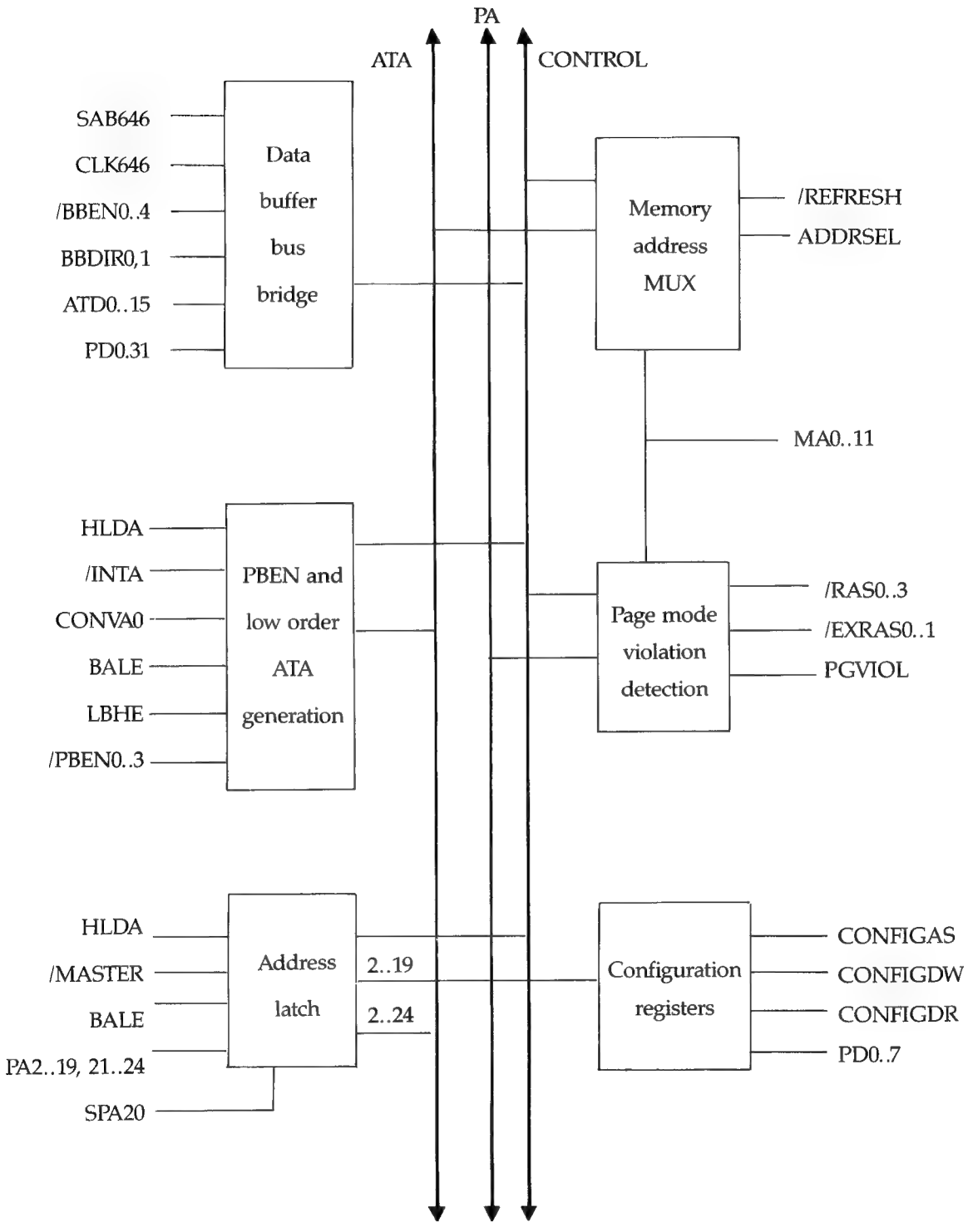


Figure 7-1. HT133 Bus Bridge Interface, Block Diagram

7.3 HT133 BUS BRIDGE INTERFACE-PINOUTS

The pin connections for the *HT133 Bus Bridge* are shown in Figure 7-2. The pins are numbered sequentially in a counter-clockwise direction from the index mark as viewed from the botton of the chip.

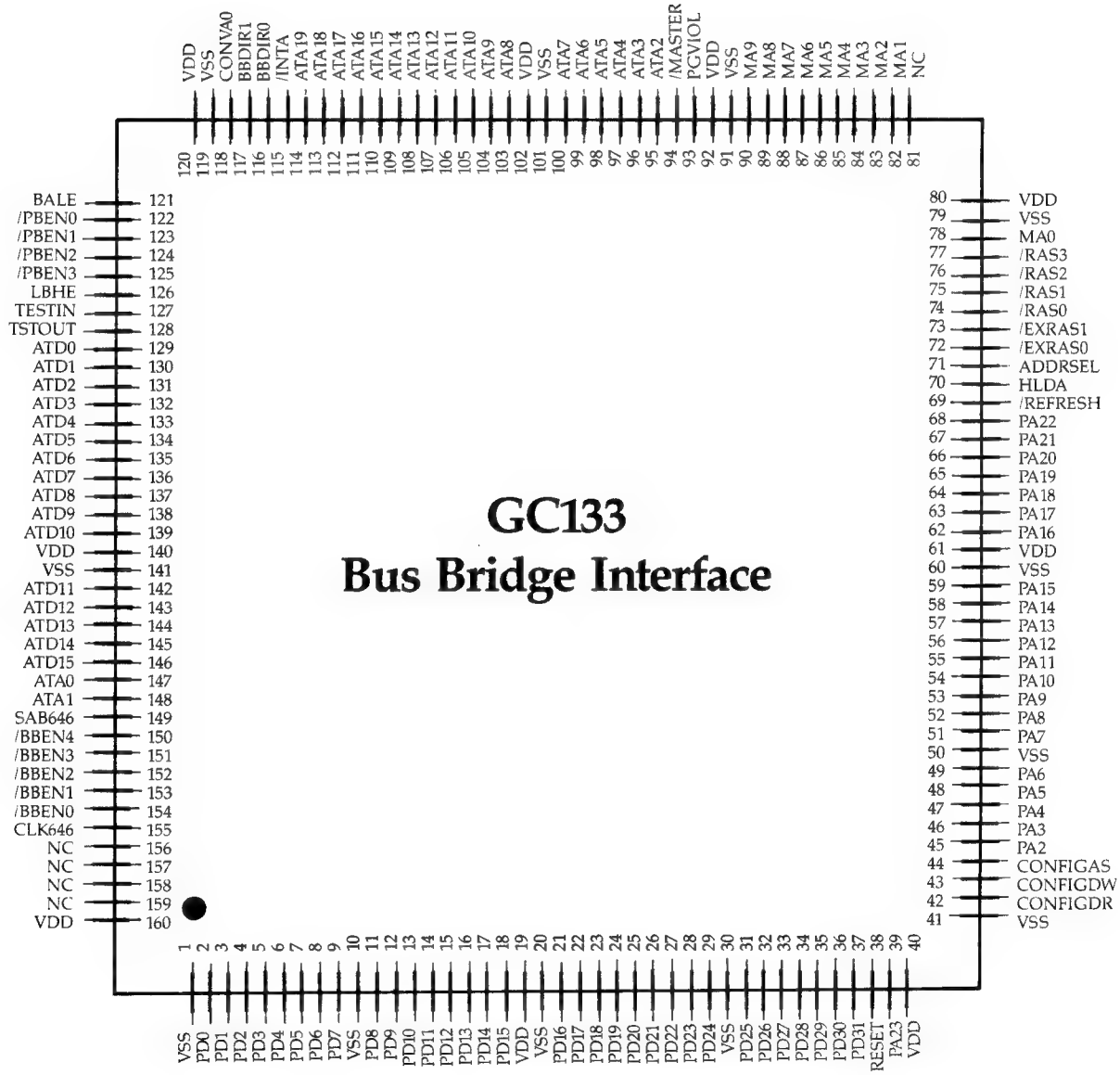


Figure 7-2. HT133 Bus Bridge Interface Pinouts

7.4 HT133 BUS BRIDGE INTERFACE PIN DESCRIPTIONS

This section describes the pins of the *HT133 Bus Bridge Interface*. The pin identification numbers correspond with those shown in *Figure 7-2 — Pinous, HT133 Bus Bridge Interface.*

Pin Symbol	Pin Number	Pin Type	Description
ADDRSEL	71	I	**Address Multiplexer Selector:** When LOW the *HT133* places ROW addresses on the MA lines, when HIGH the COLUMN addresses are on the MA lines.
ATA0 to ATA19	147 to 148 & 95 to 100 & 103 to 114	I/O	**AT Backplane Address lines:** A latched version of the PA2 to PA16 lines.
ATD0 to ATD15	129 to 139 & 142 to 146	I/O	**AT Backplane Data lines:** 16-bit data lines derived from the 32-bit processor data bus LD0-31. These lines drive the AT slots.
BALE	121	I	**Bus Address Latch Enable:** When HIGH the addresses from the processor side (PA's) are driven through to the AT side (ATA's). The trailing edge of BALE holds the current value of the address on the AT side allowing the processor addresses to change for pipeline operation.
BBDIR0, BBDIR1	116, 117	I	**Bus Bridge Direction 0:** Controls the direction of data for the bridging action between ATD0-7 and ATD8-15. When HIGH, data is bridged from lower to higher bytes on the AT side: when LOW, from upper to lower. **Bus Bridge Direction 1:** Controls the direction of data flow from the processor side to the AT side. When HIGH, data flows from the processor to the AT data bus. (During an I/O write BBDIR1 = '1'.) When LOW, data flows from the AT side to the processor side. (During an I/O read BBDIR1 = '0'.)
/BBEN0 to /BBEN3	154 151	I	**Bus Bridge Enable:** When active, indicates the byte that the *HT133* should drive — where BBEN0 is the lowest order byte and BBEN3 the highest. For example: an I/O byte READ from port 0 has BBEN0 active; *HT133* drives data onto the processor's data bus (lower byte) from the AT data bus (lower byte) 0.

Pin Symbol	Pin Number	Pin Type	Description
/BBEN4	150	I	**Bus Bridge Enable 4:** When active, enables the bridging buffer between ATD0-7 and ATD8-15. This routes the data from lower to upper bytes on the AT data bus and *viceversa*.
CLK646	155	I	**Clock LS646 Megafunction:** On the rising edge of this signal, *HT133* latches data on lines ATD0-7 and, if the direction and SAB646 is correct, presents the data to the processor's lower 8 bits.
CONFIGAS	44	I	**Configuration Address Strobe:** The new configuration INDEX is strobed on the trailing edge of this signal.
CONFIGDR	42	I	**Configuration Data Read:** If the INDEX is set within the range 10h to 1Fh, *HT133* will place the indexed register's value on the processor's data bus. If the range is set within 0h to 0Fh, HT133 does not drive the processor data bus at all — INDEX indicates a value for the *HT132 Controller*. If the range is within 40h to 4Fh, HT133 lets the data come in from the AT data bus — *HT131* is driving the bus.
CONFIGDW	43	I	**Configuration Data Write:** On the trailing edge of this signal, data on the processor's data bus is written to the indexed register (if within the range 10h to 1Fh).
CONVA0	118	I	**Conversion Cycle A0:** When this signal is active, *HT133* forces a '1' onto ATA0. This is used during 8- to 16-bit conversion cycles.
/EXRAS0 /EXRAS1	72, 73	I	**RAS signals for Banks 4 and 5:** *HT133* uses these signals to latch the latest 'page value' for the DRAMs. Used in PGVIOL calculations.
HLDA	70	I	**Hold Acknowledge:** When the DMA controller or 'MASTER' holds the bus (and the processor has granted it) this signal is active. Controls the generation of A0, A1 and LBHE signals.
/INTA	115	I	**Interrupt Acknowledge:** When active, *HT133* allows the interrupt vector flow from the AT data bus to the LOW byte on the processor bus.

Pin Symbol	Pin Number	Pin Type	Description
LBHE	126	I/O	**Latched Byte High Enable:** When active, indicates that valid data is on the high part of the 16-bit data lines.
MA0 to MA9	78, 82-90	O	**Multiplexed addresses** (DRAMs).
/MASTER	94	I	**MASTER Mode Request:** When active and in conjunction with DMA, indicates that a peripheral board (on the backplane) is driving 'address', 'commands', 'refresh', and 'data'.
PA2 to PA16	45-49, 51-59, 62.	I/O	**Processor Address (Lower and Upper) lines 2-22:** These lines are latched to form the AT Address lines. They are used to generate the MA lines for the DRAM.
PA17 to PA22	63 to 68	I	
PA23	39	I	
PA24	156	I	
/PBEN0 to /PBEN3	122 to 125	I/O	**Processor Byte Enables:** Indicates the byte on which there is valid data. Used to generate A0, LBHE and A1. Normally an input; but, during DMA is an output.
PD0 to PD31	2-9, 11-18, 21-29, 31-37	I/O	**Processor Data Lines.**
PGVIOL	93	O	**Page Violation:** This signal is the result of a COMPARE of the current address 'row' and the 'row' latched into the DRAMs. When HIGH it indicates that the two are different — thus allowing the processor access beyond the page boundary.
/RAS0 to /RAS3	74 to 77	I	**Row Address Strobe:** *HT133* uses these signals to latch the latest 'page value' for the DRAMs. Used in PGVIOL calculations.
/REFRESH	69	I	**/REFRESH:** Indicates that the current HLDA cycle is a DRAM refresh and the refresh addresses are on ATA0-11.
RESET	38	I	**RESET:** Initializes all internal registers to a known value.

Pin Symbol	Pin Number	Pin Type	Description
SAB646	149	I	**Select Transparent or Latched Data:** When LOW the *HT133 Bus Bridge* lets data flow from, transparently, the processor to the AT bus. When HIGH, *HT133 Bus Bridge* presents the latched data on the next memory READ.
TESTIN	127		**Factory test pin:** To be connected to ground.
TSTOUT	128	O	**Test Output:** Used for factory verification of chip integrity.
VDD	19, 40, 61, 80, 92, 102, 120, 140, 160	5 Volts	
VSS	1, 10, 20, 30, 41, 50 60, 79, 91, 101, 119, 141	Ground	

8

CONFIGURATION REGISTERS OF THE GCK131 CHIP SET

8.1 INTRODUCTION

This chapter describes and explains the uses of the configuration modules contained in GCK131 chip set.

8.2 GENERAL DESCRIPTION

The programmable configuration-bit registers in each of the three chips allow the GCK131 chip set to be used in a wide variety of applications. The registers are designed for use with software which, as determined by the system designer, allows the end-user some flexibility in the way the system operates. The programmable registers of each chip are:

- The GC131 Peripheral Controller configuration registers are used to select the Backplane, Refresh, and DMA clock speeds- divisions of the system clock timing- are received by the GC131 Controller. Mapping of the serial and parallel ports can be configured either by a register in the GC131, or from EEPROM control lines.

- The GC132 CPU/Memory Controller configuration registers control; the general bus timing relationship for RAM and I/O, the size of the RAM and ROM block (which can be selected by registers in the GC132 Controller), and lastly through general setup bits, control such functions as PARITY, COPROCESSOR selection, ROM SHADOWING, and the REMAPPING features.

- The GC133 Bus Bridge Interface has configuration bits that; select the DRAM configuration, control interleaving and REMAP, and also identify the chip number from a READ ONLY register within the chip. The revision number is important for system developers-it provides a method of identifying the features available in the chip set.

The Configuration Registers are Partitioned

The configuration registers of the chip set are partitioned into regions: each is non-overlapping and unique.

- I/O address 24h is a 'write-only' register within which is replaced a 'pointer' to the required INDEX.
- I/O address 28h is a 'read/write' port within which the data for the INDEX is placed.

How to Read or Write to the Registers

It is a two step process to read from or write to the registers:

1. Write the INDEX of the desired register to address 24h.
2. Read/Write the data from/to address 28h.

Each chip has its own INDEX space (or region), as follows:

- The GC132 INDEX space resides from 00h to 0Fh.
- The GC133 INDEX space resides from 10h to 1Fh.
- The GC131 INDEX space resides from 40h to 4Fh.

Signals Associated with the Configuration Registers

CONFIGAS

When an I/O WRITE is made to register 24h, CONFIGAS goes active (high) and, on the falling edge of the signal, latch the data (the INDEX pointer) on the lower either data lines into the INDEX registers of each chip of the set.

CONFIGDW

When the I/O WRITE is made to port 28h, CONFIGDW goes active (high) indicating that valid data is available on the lower eight bits of the data buses. The target chip-identified as having the INDEX register by the prescribed Region spaces noted earlier-strobes the data to the appropriate configuration register on the falling edge of CONFIGDW.

CONFIGDR

When the I/O READ to port 28h occurs, CONGIGDR goes active (high) and data will be presented to the lower eight bit of the data bus. Only one chip responds: the one whose INDEX register value matches with the proscribed range.

8.3 THE INDEXES REGISTERS

Summary of the INDEXES

Registers of the *HT132 CPU/Memory Controller*	
INDEX 00h	General setup bits
INDEX 01h	General setup bits
INDEX 02h	High speed override bits
INDEX 03h	DRAM configuration
INDEX 04h	DRAM configuration (Banks 0, 1, 2, 3)
INDEX 05h	DRAM configuration (Banks 4, 5)
INDEX 06h to INDEX 09h	Tailoring timing requirements
An Example	AT standards
INDEX 06h	EPROM configuration
INDEX 07h	I/O Channel RAM Configuration
INDEX 08h	I/O access configurations
INDEX 09h	Interrupt acknowledge configurations
INDEX 0Ah-0Bh	Test registers
INDEX 0Ch	Identification register
INDEX 0Dh	Optional Configuration -1
INDEX 0Eh	Optional Configuration -2
INDEX 0Fh	Optional Configuration -3

Registers of the *HT133 Bus Bridge Interface*	
INDEX 10h	DRAM configurations
INDEX 11h	Reserved
INDEX 12h	Reserved
INDEX 13h	Revision identification

Registers of the *HT131 Peripheral Controller*	
INDEX 40h	Clock dividers for low speed
INDEX 41h	Clock dividers for high speed
INDEX 42h	DMA and REFRESH wait states
INDEX 43h	Serial parallel and mapper selections
INDEX 44h	Video external register strobe
INDEX 45h	EEPROM Control
INDEX 46h	Reserved
INDEX 47h	Revision identification
INDEX 48h	MODE Reconfiguration
INDEX 49h	Additional REFRESH Wait states
INDEX 92h	PORT — FAST_RC and ALT_MUX PA20

INDEX00h — General setup bits

Default value = 00h
The configuration bits of INDEX00h are available for programming general system setup.
Coprocessor (Bits 0 and 1)
Bit 0 toggles to enable or disable the numeric coprocessor (if installed).
The default (Bit 0 = '0') applies if the system is not fitted with the device.
Use Bit 1 to indicate the device type. The default (Bit 1 = '0') indicates an 80387 device. If an 80287 is fitted, Bit 1 is set equal to '1'.
Parity check (Bit 3)
The default setting (Bit 3 = '0') selects parity checking OFF.
DRAM banks 4 and 5
As required to match the installed devices, use Bit 4 to enable or disable the use of DRAM Banks 4 and 5.
Lower and Middle BIOS
As detailed in a previous chapter 6.3 (*'Programming the configuration registers'),* Use Bits 6 and 7 to enable the shadowing of the lower and/or middle BIOS images of BIOS into DRAM.

Bit	State	Description
0	= 0	Coprocessor, disabled.
	= 1	Coprocessor, enabled.
1	= 0	Coprocessor type = 80387
	= 1	Coprocessor type = 80287
2	= 0	Reserved. Should always be programmed to 0.
3	= 0	Parity, disabled.
	= 1	Parity, enabled.
4	= 0	DRAM Banks 4 and 5, disabled.
	= 1	DRAM Banks 4 and 5, enabled.
5	= 0	CAS Shift, disabled.
	= 1	CAS Shift, enabled. NOTE: CAS will be delayed by one-half FAST 'CLK2' cycle during a WRITE operation — to accommodate slow processors.
6	= 0	Lower BIOS, Not shadowed.
	= 1	Lower BIOS, Shadowed into DRAM.
7	= 0	Middle BIOS, Not shadowed.
	= 1	Middle BIOS, Shadowed into DRAM (If present).

Figure 8-1. INDEX001h, General Setup Bits

INDEX01h — General setup bits

Default value = 88h
The configuration bits of INDEX01h are also available for general system setup purposes. As indicated below, use Bit 0 to enable or disable the shadowing of Video BIOS. Use Bit 1 to control the use of PAGE mode. The BIOS EPROM type is selected by Bit 2.
Other Bits are used in this manner;
Use Bit 3 to select the 80387 coprocessor CLOCK mode as either asynchronous or synchronous. Video BIOS shadowing is selected either OFF or ON by Bit 4. Similarly, Bit 5 controls the REMAP, Bit 6 enables or disables the use of Middle BIOS (*).

Bit	State	Description
0	= 0	Video BIOS, Not shadowed into DRAM.
	= 1	Video BIOS, Shadowed into DRAM.
1	= 0	Page mode, disabled.
	= 1	Page mode, enabled.
2	= 0	BIOS EPROM type = 27256
	= 1	BIOS EPROM type = 27512
3	= 0	CLOCK mode (80387), asynchronous.
	= 1	CLOCK mode (80387), synchronous.
4	= 0	Video BIOS shadowing, disabled.
	= 1	Video BIOS shadowing, enabled.
5	= 0	REMAP (above 1, 2, or 4 Mb), disabled.
	= 1	REMAP (above 1, 2, or 4 Mb), enabled.
6	= 0	Middle BIOS, disabled.
	= 1	Middle BIOS, enabled.
7	= 0	Quiet bus, disabled.
	= 1	Quiet bus, enabled. During high-speed local access, the commands are not issued to the backplane. And BALE is kept HIGH during the cycle.

Figure 8-2. INDEX01h, General Setup Bits (Continued)

INDEX02h — High speed override bits

Default value = FFh
Use these configuration bits if high speed SRAMs **are installed in preference to** DRAMs in one or more banks of the system. Each bank can be individually configured to optimize system performance.
When the override bit for a particular bank is ON, the 'forced' delays indicated in Figure 8c are used rather than the programmed values of INDEX04h and 05h.

Bit	State	Description
0	= 0	DRAM delay BANK 0, override ON; **forces these delays:** 0 RAS delays, 2 CAS delays, 2 CAS active, RECOVERY, PAGE VIOLATIONS are always 'false'.
	= 1	DRAM delay BANK 0, override OFF; acts on the settings of INDEX04h and 05h.
1	= 0	DRAM delay BANK 1, override ON.
	= 1	DRAM delay BANK 1, override OFF.
2	= 0	DRAM delay BANK 2, override ON.
	= 1	DRAM delay BANK 2, override OFF.
3	= 0	DRAM delay BANK 3, override ON.
	= 1	DRAM delay BANK 3, override OFF.
4	= 0	DRAM delay BANK 4, override ON.
	= 1	DRAM delay BANK 4, override OFF.
5	= 0	DRAM delay BANK 5, override ON.
	= 1	DRAM delay BANK 5, override OFF.
6	= 0	Reserved. Always program to '0'.
7	= 0	Reserved. Always program to '0'.

Figure 8-3. INDEX02h, High-Speed Override Bits

INDEX03h — DRAM configuration

Default value = A0h
This configuration register is used to **match the number and type of DRAMs** used in the system. The selection of either 256K or 1 Mb DRAMs is made within two groups; namely, Banks 0, 1 and Banks 2 through 5. This arrangement does not allow the intermixing of DRAM types — *See the Note (*) regarding INDEX10h.*
Interleaving and EMS PAGE address settings are also configured using this configuration register.

Bit	State		Description
0,1	**Bit 0**	**Bit 1**	*The combination of Bits 0 and 1 select the following:*
	= 0	= 0	DRAMs are 256K.BANK0 through BANK5.
	= 0	= 1	Reserved.
	= 1	= 0	Reserved.
	= 1	= 1	DRAMs are 1 Mb. BANK0 through BANK5.
3,2	**Bit 3**	**Bit 2**	*The combination of Bits 3 and 2 select the following:*
	= 0	= 0	One bank of DRAM enabled, interleave OFF.
	= 0	= 1	Two banks of DRAM enabled, interleave ON.
	= 1	= 0	Not permitted.
	= 1	= 1	Four banks of DRAM enabled, interleave ON.
7 6 5 4	See Descr-iption.		**EMS page.** The settings of Bits 7 through 4 specify a 64k 'hole' of 'OFFBOARD' RAM (not DRAM) starting at the coded value. The default settings are: Bit 7 = 1, Bit 6 = 0, Bit 5 = 1, Bit 4 = 0; meaning, '1010'. This translates to a 64k EMS hole that starts at *A0000h*.

Figure 8-4. INDEX03h, DRAM Configuration

Note: In conjunction with the setting of INDEX03h used to select the use of either 256K or 1 Mb DRAMs, INDEX10h must also be similarly programmed. If not done, the system will not operate properly.

INDEX04h — DRAM configuration (Banks 0, 1, 2, 3)

Default value = FFh
This configuration register is available to set up the timing of RAS and CAS signals to the DRAMS for Banks 0 through 3.

The delays (shown below) are programmed as multiples of CLKIN cycles.
RAS delay is measured from the rising edge of CLKIN during/ADS active.

The register settings, as programmed with INDEX04h, are used for Banks 0 through 3 of the system *unless* (by INDEX02h) overrides have been selected for one or more banks.

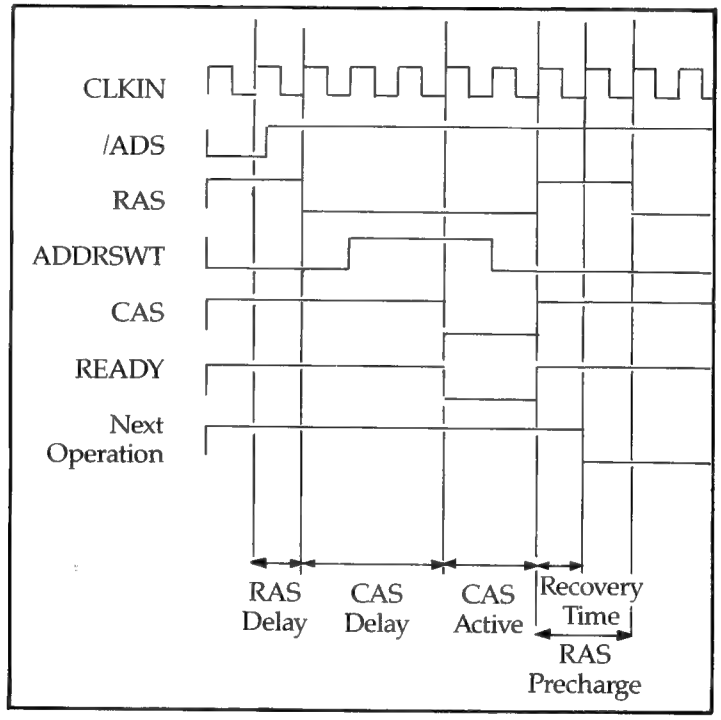


Figure 8-5. DRAM Timing, as Referenced in INDEX04

Bit	State		Description
1, 0	**Bit 1**	**Bit 0**	*The combination of Bits 1 and 0 select the following:*
	= 0	= 0	Zero RAS delay.
	= 0	= 1	One RAS delay.
	= 1	= 0	Two RAS delays.
	= 1	= 1	Three RAS delays.
2	= 0		Two CAS delays measured from RAS in CLKIN.
	= 1		Three CAS delays.

Bit	State		Descriiption
6, 3	**Bit 6**	**Bit 3**	*The combination of Bits 6 and 3 select the following:*
	= 0	= 0	Two CAS active CLKIN cycles.
	= 0	= 1	Four CAS active.
	= 1	= 0	Six CAS active.
	= 1	= 1	Eight CAS active.
4	= 0		Four RAS precharge CLKIN cycles.
	= 1		Six RAS precharge.
5	= 0		Zero recovery time.
	= 1		Two recovery CLKIN cycles.

Figure 8-6. INDEX04h, DRAM Timing BANKS0...3

INDEX05h — DRAM configuration (Banks 4, 5)

Default value = FFh
This configuration register is available to program the timing for RAS and CAS in Banks 4 and 5. [HINT: See *INDEX04h* for more information about delay timing.]

Bit	State		Description
1, 0	**Bit 1**	**Bit 0**	*The combination of Bits 1 and 0 select:*
	= 0	= 0	Zero RAS delays.
	= 0	= 1	One RAS delay measured in CLKIN cycles.
	= 1	= 0	Two RAS delays.
	= 1	= 1	Three RAS delays.
2	= 0		Two CAS delays measured from RAS in CLKINS.
	= 1		Three CAS delays.
6, 3	**Bit 6**	**Bit 3**	*The combination of Bits 6 and 3 select:*
	= 0	= 0	Two CAS active CLKINs.
	= 0	= 1	Four CAS active.
	= 1	= 0	Six CAS active.
	= 1	= 1	Eight CAS active.
4	= 0		Four RAS precharge CLKINs.
	= 1		Six RAS precharge.
5	= 0		Zero recovery time.
	= 1		Two recovery CLKINs.

Figure 8-7. INDEX05h, DRAM Timing for BANKS 4 and 5

INDEX06h to INDEX09h — Tailor timing requirements

The configuration registers INDEX06h through 09h are available to tailor the timing requirements for various system commands.
Delays are given as CLKIN cycles.
On the following pages, Figure 8-8 through 7m for configuration registers INDEX06h through 09h indicate various 'delays'. These delays are multiples of CLKIN cycles. Figure 8-9 diagrams their relationships.

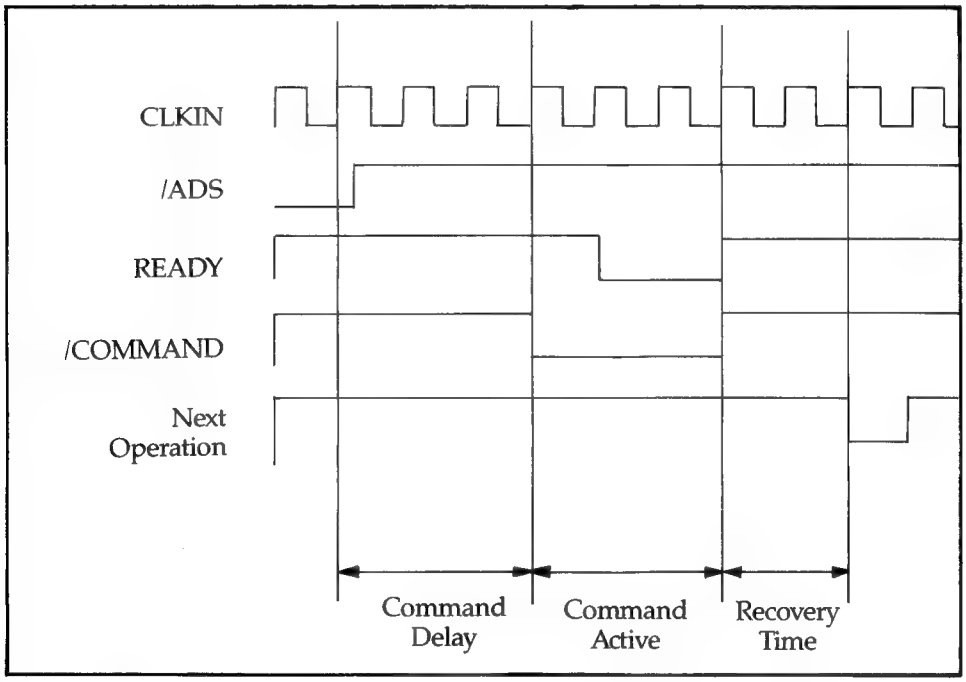


Figure 8-8. Cycle Timing, as Referenced in INDEX06h to 09h

An example

Objective:
In this example, we wish to match the I/O timing of the *GCK131 Chip Set* (operating at 25MHz) with a 'generic' system that uses the AT-standard (running at 8MHz).

At-standards:
As a first step, the generic I/O timing values of the AT are used to give values useful in programming the *GCK131 Chip Set*. Figure 8.9 illustrates these relationships.

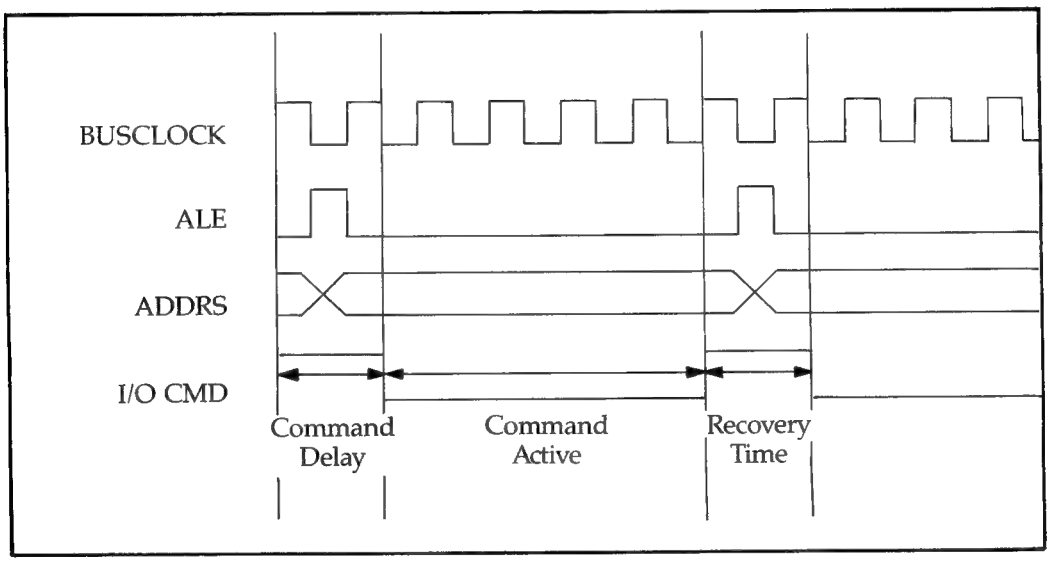


Figure 8-9. Generic AT-System I/O Timing, 3-Wait States

(i) With a BUSCLOCK frequency (F) of 8MHz: the period (T) is 125ns.

(ii) With 4 wait states inserted: the total I/O command active time (4.5×125ns) is 560ns.

(iii) The command delay (1.5×T) is 200ns.

(iv) The recovery time (1.5×T) is 200ns.

The chip timing relationships of the *CGK131 Controller* are referenced as multiples of CLKIN which, at 25MHz, means the oscillator beats at 50MHz.

(v) The reciprocal (t) — or, 1 divided by 50MHz — is 20ns.
Thus,

(vi) For a command active time of 560ns we require 28 CLKINS (560ns divided by 20ns).

(vii) For a command delay of 200ns we require 10 CLKINS (200ns divided by 20ns).

(ix) For a recovery time of 200ns we require 10 CLKINS (200ns divided by 20ns).

To match the generic 8 Mhz timing for I/O access — and 4 wait states — we program the INDEX08h (I/O Access) configuration register as follows:

(a) For a command delay of 10 CLKINS (*paragraph vii*);
INDEX08h, Bit 1 = '0', Bit 0 = '0'.

(b) For a command active period of 28 CLKINS (paragraph vi);
INDEX08h, Bit 3 = '1', Bit 2 = '0'.

(c) For a recovery time of 10 CLKINS (*paragraph ix*);
INDEX08h, Bit 5 = '0', Bit 4 = '1'.

With INDEX08h, Bits 6 and 7 both programmed each as '1' the contents of **INDEX08h equals d8h.**

INDEX06h — EPROM configuration

Default value = FFh
Configuration registers INDEX06h through 09h are available to tailor the timing requirements, for various commands, of the system. An earlier example (*See INDEX06h to INDEX09h — Tailor timing requirements)*
On the following pages, Figure 8-11 through 8-14 introduce various timing relationships that can be programmed into the system. The relationships are multiples of CLKIN cycles. Figure 8-9 diagrams the relationships.

Bit	State		Description
0	= 0		Three command delays in CLKINS.
	= 1		Five command delays.
2,1	**Bit 2**	**Bit 1**	*The combination of Bits 2 and 1 select the following:*
	= 0	= 0	Eight command active times in CLKINS.
	= 0	= 1	Ten command active times.
	= 1	= 0	Twelve command active times.
	= 1	= 1	Fourteen command active times.
4, 3	**Bit 4**	**Bit 3**	*The combination of Bits 4 and 3 select the following:*
	= 0	= 0	Two RECOVERY times in CLKINS.
	= 0	= 1	Four RECOVERY times in CLKINS.
	= 1	= 0	Six RECOVERY times in CLKINS.
	= 1	= 1	Eight RECOVERY times in CLKINS.
5	= 1		Reserved. Always program to '1'.
6	= 1		Reserved. Always program to '1'.
7	= 1		Reserved. Always program to '1'.

Figure 8-10. INDEX06h, EPROM Configuration

INDEX07h — I/O Channel RAM configuration

Default value = FFh
Configuration registers INDEX06h through 09h are available to tailor the timing requirements, for various commands, of the system. An earlier example (*See INDEX06h to INDEX09h — Tailor timing requirements*)
The timing indicated in the following Figure is related to CLKIN cycles.

Bit	State		Description
0	= 0		Five command delays in CLKINs.
	= 1		Seven command delays.
2, 1	**Bit 2**	**Bit 1**	*The combination of Bits 2 and 1 select the following:*
	= 0	= 0	Seven command active times in CLKINs.
	= 0	= 1	Nine command active times.
	= 1	= 0	Eleven command active times.
	= 1	= 1	Thirteen command active times
4, 3	**Bit 4**	**Bit 3**	*The combination of Bits 4 and 3 select the following:*
	= 0	= 0	Zero RECOVERY times in CLKINs.
	= 0	= 1	Two RECOVERY times in CLKINs.
	= 1	= 0	Four RECOVERY times in CLKINs.
	= 1	= 1	Six RECOVERY times in CLKINs.
5	= 1		Reserved. Should always be programmed to '1'.
6	= 1		Reserved. Should always be programmed to '1'.
7	= 1		Reserved. Should always be programmed to '1'.

Figure 8-10. INDEX07h, 16-Bit RAM Configuration

INDEX08h — I/O access configurations

Default value = FFh
Configuration registers INDEX06h through 09h are available to tailor the timing requirements, for various commands, of the system. An earlier example (*See INDEX09h to INDEX09h — Tailor timing requirements*)
The timing indicated in the following Figure is related to CLKIN cycles.

Bit	State		Description
1, 0	**Bit 1**	**Bit 0**	*The combination of Bits 1 and 0 select the following:*
	= 0	= 0	Ten command delay times in CLKINs.
	= 0	= 1	Twelve command delay times
	= 1	= 0	Sixteen command delay times.
	= 1	= 1	Eighteen command delay times.
3, 2	**Bit 3**	**Bit 2**	*The combination of Bits 3 and 2 select the following:*
	= 0	= 0	Eighteen command active times in CLKINs.
	= 0	= 1	Twenty-two command active times in CLKINs.
	= 1	= 0	Twenty-eight command active times in CLKINs.
	= 1	= 1	Thirty-four command times in CLKINs.
5, 4	**Bit 5**	**Bit 4**	*The combination of Bits 5 and 4 select the following:*
	= 0	= 0	Eight RECOVERY times in CLKINs.
	= 0	= 1	Ten RECOVERY times in CLKINs.
	= 1	= 0	Fourteen RECOVERY times in CLKINs.
	= 1	= 1	Sixteen RECOVERY times in CLKINs.
6,	= 1		Reserved. Should always be programmed to '1'.
7	= 1		Reserved. Should always be programmed to '1'.

Figure 8-11. INDEX08h, I/O Access Configuration

INDEX0Ch — Identification register

INDEX0Ch is a READ-ONLY register which, at system power-up, defaults to a value of '02h', It can be used, if incorporated into BIOS routines, to identify the 'revision' of the installed *HT132 Controller*.

Bit		Usage
	7654 3210	
0....7	0000 0010	Indicates the revision identification for BIOS programmers.

Figure 8-12. Identification Register

INDEX0Dh — [OPTCNFG1]

IINDEX0Dh is a READ/WRITE register which, at system power-up, defaults to a value of '00h'. The register is available for programming as the means to adjust the 16-bit timing features of the Revision 'C' chip.

Bit	State		Usage
0	= 0		8-bit timing for Backplane accesses.
	= 1		Enables programmable 16-bit timing for Backplane accesses.
2, 1	**Bit 2**	**Bit 1**	
	= 0	= 0	7 CLKIN periods, 'Command Active' for 16-bit RAM.
	= 0	= 1	9 CLKIN periods.
	= 1	= 0	11 CLKIN periods.
	= 1	= 1	13 CLKIN periods.
4, 3	**Bit 4**	**Bit 3**	
	= 0	= 0	18 CLKIN periods, 'Command Active' for 16-bit I/O.
	= 0	= 1	22 CLKIN periods.
	= 1	= 0	28 CLKIN periods.
	= 1	= 1	34 CLKIN periods.
6, 5	**Bit 6**	**Bit 5**	
	= 0	= 0	10 CLKIN periods, 'Command Delay' for 16-bit I/O.
	= 0	= 1	12 CLKIN periods.
	= 1	= 0	16 CLKIN periods.
	= 1	= 1	18 CLKIN periods.
7	= 0		Compatible with Rev. 'B' chips.
	= 1		Enables FAST page-mode on-board DRAM access.

Figure 8-13. Optional Configuration-1

INDEX0Eh — [OPTCNFG2]

INDEX0Eh is a READ/WRITE register which, at system power-up, defaults to a value of '00h'. The register is available for programming as the means to use and adjust features of the Revision 'C' chip.

Bit	State		Usage
1, 0	Bit 1	Bit 0	
	= 0	= 0	1 CLKIN period, 'Command Advance' for /MEMW and /IOW.
	= 0	= 1	2 CLKIN periods.
	= 1	= 0	3 CLKIN periods.
	= 1	= 1	1 CLKIN period.
2	= 0		Compatible with Revision 'B' chips.
	= 1		The RC signal is blocked until HLDA is inactive.
3	= 0		Compatible with Revision 'B' chips.
	= 1		The SHUTDOWN cycle begins after the DRAM cycle is completed.
4	= 0		Compatible with Revision 'B' chips.
	= 1		Enable the DRAM interleave fix.
5	= 0		Compatible with Revision 'B' chips.
	= 1		Enable the Quiet bus PARITY fix.
6	= 0		Allows the software CO-PROC reset.
	= 1		Blocks the software CO-PROC reset.
7	= 0		Compatible with Revision 'B' chips RESET387 = CLREXPTION.
	= 1		RESET387 = CLREXPTION on powerup only.

Figure 8-14. Optional Configuration-2

INDEX0Fh — [OPTCNFG3]

INDEX0Fh is a READ/WRITE register which, at system power-up, defaults to a value of '00h'. The register is available for programming as the means to use and adjust features of the Revision 'C' chip.

Bit	State	Usage
0	= 0	BS16 is compatible with Revision 'B' chips.
	= 1	The BS16 signal is removed after each cycle.
1	= 0	BS32 is compatible with Revision 'B' chips.
	= 1	The BS32 blocks all but local accesses.
2	= 0	Video BIOS resides in the lower 32Kb chunk (in the range C0000h to C7FFFh). (See *'Video BIOS space in Window I can be split'* on Page 89).
	= 1	Video BIOS resides in the upper 32Kb chunk (in the range C8000h to CFFFFh).
3	= 0	Video BIOS is (in size) 64Kb.
	= 1	Video BIOS is (in size) 32Kb. (See *'Video BIOS space in Window I can be split'* on Page 89)
4	= 0	Reserved. Always program to '0'.
	= 1	Illegal.
5	= 0	Enables 1 extra clock cycle between ADDSEL and/CAS during DMA cycles.
	= 1	Disables the extra clock cycle between ADDSEL and /CAS during DMA cycles.
6	= 0	The /LOCAL signal is latched. Compatible with Revision 'B' chips.
	= 1	The /LOCAL signal is allowed to flow through.
7	= 0	Compatible with Revision 'B' chips.
	= 1	'BALE' is held LOW during 'quiet bus' local accesses.

Figure 8-15. Optional Configuration-3

INDEX09h — Interrupt acknowledge configurations

Default value = FFh
Configuration registers INDEX06h through 09h are available to tailor the timing requirements, for various commands, of the system. An earlier example (*See INDEX06h to INDEX09h — Tailor timing requirements)*
The timing indicated in the following Figure is related to CLKIN cycles.

Bit	State		Description
0	= 0		Three command delay times in CLKIN cycles.
	= 1		Three command delay times in CLKINs.
2, 1	**Bit 2**	**Bit 1**	*The combination of Bits 2 and 1 select the following:*
	= 0	= 0	Five command active times in CLKINs.
	= 0	= 1	Seven command active times.
	= 1	= 0	Nine command active times.
	= 1	= 1	Eleven command active times.
3	= 0		Two RECOVERY times in CLKINs.
	= 1		Four RECOVERY times in CLKINs.
4,	= 1		Reserved. Should always be programmed to '1'.
5,	= 1		Reserved. Should always be programmed to '1'.
6,	= 1		Reserved. Should always be programmed to '1'.
7	= 1		Reserved. Should always be programmed to '1'.

Figure 8-16. INDEX09h, Interrupt Acknowledge Configuration

INDEX0Ah through 0Fh are Test registers

Indices 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, and 0Fh are test registers and should not be used.

INDEX10h — DRAM configurations

Default value = 00h
This configuration register is available for programming the number and type of DRAMs used in the system — *See Note (*)*. It is also used the enable or disable the REMAP and interleave options — as programmed with INDEX03h.

Bit	State		Description
0, 1	**Bit 0**	**Bit 1**	*The combination of Bits 0 and 1 select the following:*
	= 0	= 0	DRAMs are 256K. BANK0 through BANK5.
	= 0	= 1	Reserved.
	= 1	= 0	Reserved.
	= 1	= 1	DRAMs are 1 Mb. BANK0 through BANK5.
2	= 0		1 DRAM bank, interleave OFF.
	= 1		2, 4, or 6 banks of DRAM, auto-interleave ON.
3	= 0		Disable 384K, REMAP above 1, 2, or 4 Mb.
	= 1		REMAP, enable.
4,	= 0		Reserved. Always program to '0'.
5,	= 0		Reserved. Always program to '0'.
6,	= 0		Reserved. Always program to '0'.
7	= 0		Reserved. Always program to '0'.

Figure 8-17. INDEX10h, DRAM Configuration

Note: In conjunction with the setting of INDEX10h used to establish the use of either 256K or 1 Mb DRAMs, INDEX03h must also be similarly programmed. If not done, the system will not operate properly.

INDEX11 — RESERVED

INDEX12 — RESERVED

INDEX13h — Revision identification

The contents of INDEX13h are available for use in programming when the objective is to determine the availability — by reference to the revision number — of the *GCK131 Chip Set* features.
This document is issued concurrently with the release of chips identified '01' in INDEX13h. Revised versions of the *GCK131 Chip Set* will be identified in INDEX13h in the sequence '02, 03...'. For more information, contact your G2 Incorporated representative.

Bit	State	Description
7 to 0	01h	Revision ID.

Figure 8-18. INDEX13h

INDEX40h — Clock dividers for low speed (non-TURBO mode)

Default value = 10h
INDEX40h is available to program the desired clock rates for various functions of the *GCK131 Chip Set* when operating in non-TURBO mode.(*) The resultant clock rate is a division of the incoming signal at the '/SYSCLK' input.
Bits 0 and 1 control the frequency of BUSCLOCK to the backplane. Bits 2 and 3 are used to select the desired REFRESH speed. Similarly Bits 4 and 5 program the DMA speed while in non-TURBO mode.

Bit	State		Description
1, 0	**Bit 1**	**Bit 0**	*The combination of Bits 1 and 0 select the following:* Back plane (BUSCLOCK) clock divider for SLOW speed.
	= 0	= 0	Divide incoming/SYSCLK by one.
	= 0	= 1	Divide incoming/SYSCLK by two.
	= 1	= 0	Divide incoming/SYSCLK by four.
	= 1	= 1	Divide incoming/SYSCLK by eight.
3, 2	**Bit 3**	**Bit 2**	*The combination of Bits 3 and 2 select the following:* REFRESH clock divider for SLOW speed.
	= 0	= 0	Divide incoming/SYSCLK by one.
	= 0	= 1	Divide incoming/SYSCLK by two.
	= 1	= 0	Divide incoming/SYSCLK by four.
	= 1	= 1	Divide incoming/SYSCLK by eight.

Figure 8-19. INDEX40h, Clock Dividers (Non-TURBO Mode)

Bit	State		Description
5, 4	**Bit 5**	**Bit 4**	*The combination of Bits 5 and 4 select the following:* DMA clock divider for SLOW speed.
	= 0	= 0	Divide incoming/SYSCLK by one.
	= 0	= 1	Divide incoming/SYSCLK by two.
	= 1	= 0	Divide incoming/SYSCLK by four.
	= 1	= 1	Divide incoming/SYSCLK by eight.
6, 7	= 0		Reserved. Always program to '0'.
	= 0		Reserved. Always program to '0'.

Figure 8-19. INDEX40h, Clock Dividers (Non-TURBO Mode)

Note: For information regarding TURBO mode — See INDEX4lh. Indicated FAST/SLOW (Pin 130) of the GC131 Controller.

INDEX41h — Clock dividers for high speed (TURBO)

Default value = 3Ah
INDEX41h is available to program the desired clock rates for various functions of the *GCK131 Chip Set* when operating in TURBO mode.(*) The resultant clock rate is a division of the incoming signal at the '/SYSCLK' input.
Bits 0 and 1 control the frequency of BUSCLOCK to t he backplane. Bits 2 and 3 are used to select the desired REFRESH speed. Similarly Bits 4 and 5 program the DMA speed while in TURBO mode.

Bit	State		Description
1, 0	**Bit 1**	**Bit 0**	*The combination of Bits 1 and 0 select the following:* Back plane (BUSCLOCK) clock divider for FAST speed.
	= 0	= 0	Divide incoming/SYSCLK by one.
	= 0	= 1	Divide incoming/SYSCLK by two.
	= 1	= 0	Divide incoming/SYSCLK by four.
	= 1	= 1	Divide incoming/SYSCLK by eight.
3, 2	**Bit 3**	**Bit 2**	*The combination of Bits 3 and 2 select the following:* REFRESH clock divider for FAST speed.
	= 0	= 0	Divide incoming/SYSCLK by one.
	= 0	= 1	Divide incoming/SYSCLK by two.
	= 1	= 0	Divide incoming/SYSCLK by four.
	= 1	= 1	Divide incoming/SYSCLK by eight.

Figure 8-20. INDEX41h, Clock Dividers (TURBO Mode)

Bit	State		Description
5, 4	**Bit 5**	**Bit 4**	*The combination of Bits 5 and 4 select the following:* DMA clock divider for FAST speed.
	= 0	= 0	Divide incoming/SYSCLK by one.
	= 0	= 1	Divide incoming/SYSCLK by two.
	= 1	= 0	Divide incoming/SYSCLK by four.
	= 1	= 1	Divide incoming/SYSCLK by eight.
6,	= 0		Reserved. Always program to '0'
7	= 0		Reserved. Always program to '0'

Note: For information regarding non-TURBO mode — See INDEX40h. Indicated by FAST/SLOW (Pin 130) of the GC131 Controller.

INDEX42h — DMA and REFRESH wait states

Default value = 00h
This configuration register is available to program the number of wait states required in REFRESH and DMA operations. In use, programmers are to be advised that this index (INDEX42h) must be adjusted in a sequence after those of INDEX40h and INDEX41h.
When programming the REFRESH and DMA wait states, this INDEX42h uses a four-bit binary representation (0...15) of the number of desired wait states in multiples of the clock period programmed in INDEX40h and INDEX41h.

Bit	Description
	REFRESH wait states.
3,	A Bininary count of the number of wait states of REFRESH
2,	clock
1,	Where: Bits 3, 2, 1, 0 = 0 represent 0 wait states.
0	And, Bits 3, 2, 1, 0 = 1 represents 15 wait states.
	DMA wait states
7,	A Binary count of the number of wait states of
6,	DMA clock.
5,	Where: Bits 3, 2, 1, 0 = 0 represent 0 wait states.
4	And, Bits 3, 2, 1, 0 = 1 represents 15 wait states.

Figure 8-21. INDEX42h, DMA and REFRESH Wait States

INDEX43h — Serial, parallel and mapper selections

Default value = 00h
The *GCK131 Chip Set* has built-in decoding logic for I/O devices; including, two serial ports and one parallel port.
Serial port 1 is mapped to COM1 (3F8h...3FFh) and **serial port 2** is mapped to COM2 (2F8h...2FFh). The serial ports can be selected by Bits 0 and 1 of this INDEX43h.
The parallel port decoding can be selected — for either LPT1 (378h...37Fh) or LPT2 (278h...27Fh) — by Bit 2 of this INDEX43h.

Bit	State	Description
0	= 0 = 1	Serial port 1, disable. Serial port 1, enable.
1	= 0 = 1	Serial port 2, disable. Serial port 2, enable.
2	= 0 = 1	Parallel port, configure as LPT2. Parallel port, configure as LPT1.
3	= 0 = 1	Parallel port, disable. Parallel port, enable.
4	= 0 = 1	DMA, standard AT 8-bit page mapping. Extended DMA 16-bit page mapping, enabled NOTE: The address for the PAGE MAPPER is the same as the AT standard; but, the additional 8 bits are mapped 10h addresses above the usual location. (See Figure 7t.) If 8-bit mapping is selected, the upper addresses produce a '0' and accesses are disallowed to I/O locations 90h to 9Fh.
5, 6, 7	= 0, = 0, = 0	Reserved. Always program to '0'. Reserved. Always program to '0'. Reserved. Always program to '0'.

Figure 8-22. INDEX43h, Serial, Paralle, and Mapper Select

INDEX43h — Extended DMA 16-bit page mapping

Operation	Mapping Address A16-23h	Mapping Address A24-31h
/DACK0	87h	97h
/DACK1	83h	93h
/DACK2	81h	91h
/DACK3	82h	92h
/DACK5	8Bh	9Bh
/DACK6	89h	99h
/DACK7	8Ah	9Ah
REFRESH	8Fh	9Fh

All thirty-two 8-bit registers between 80h and 9Fh can be written and read back. If 8-bit mapping is selected in the Configuration Register then — A24h to A31h produce '00' and no access is allowed to the registers at 90h to 9Fh. The mapped addresses are, during DMA and REFRESH cycles, driven on ATA16 to ATA19 and also on LA17 to LA31.

Figure 8-23. INDEX43h, Extended DMA 16-bit Page Mapping

INDEX44h — Video external register strobe

Default value = 00h
A WRITE to this port clocks data to an internal register of the *GC131 Peripheral Controller.* It also strobes/CSVREG. The external strobe is intended to clock the data into the actual register and thus mimic the configuration switches on the video board.
When this port is read, data inside the *GC131 Controller* is driven onto the data bus. In effect, the controller provides a 'shadow' of the video configuration switches.
A READ to this port does not strobe/CSVREG.

INDEX45h — EEPROM Control

Default value = 00h
This configuration register is available for programming to control EEPROM accesses. It is possible to interface, directly, with an EEPROM device (like the *Monolithic Memories Type MC9306* device) using suitable programming.
With this register INDEX45h, interface signals of CLOCK, DATA, and CHIP SELECT can be controlled in order to READ/WRITE the EEPROM.

Bit	State	Description
0		EEPROM data IN/OUT. When data is written, it appears on pin DOEEP. When read, the data comes from pin DIEEP.
1		EEPROM clock. Data, written on this bit, appears, on pin CKEEP.
2	= 0 = 1	EEPROM chip select. Output pin CSEEP = 0. Output pin CSEEP = 1.
3, 4, 5, 6, 7	= 0 = 0 = 0 = 0 = 0	Reserved. Always program to '0'. Reserved. Always program to '0'. Reserved. Always program to '0'. Reserved. Always program to '0'. Reserved. Always program to '0'.

Figure 8-24. INDEX45h, EEPROM Control

INDEX46h — Reserved

INDEX47h — Revision Identification

Default value = 02h
This contents of READ-ONLY configuration register, INDEX47h are available for use in programming — where the objective is to determine (by referencing the Revision Number) the availability of certain *ATLAS Chip Set* features.

For more information, contact your LSI Logic representative.

Bits	State	Description
7 to 0	02h	Revision ID (READ ONLY)

Figure 8-25. INDEX47h, Revision Identification

INDEX48h — Mode reconfiguration

Default value = 00h
The *ATLAS Chip Set* has enhanced features that allow the system designer an opportunity to redefine specific I/O services at the Pin levels of the *HT131 Peripheral Controller.(*)*

Bits	State	Description		
0	= 0	Allow connection to discrete parallel ports.		
		When Bit 0 = '0'		When Bit 0 = '1' REDEFINED AS
		/PCSRPA	→	/PARCS
		/PCSWPA	→	/BFEN
		/PCSRPB	→	BFDIR
		/PCSWPC	→	/LPTOE
		/PCSRPC	→	Not Connected
		PARIE		To be strapped to VCC
	= 1	Enable direct connection with the 16C452 device (or equivalent) and provide on-board I/O buffer control signals.		
1	= 0	PORT92h functions disabled, ENP92 = '0'		
		When Bit 1 = '0'		When Bit 0 = '1' REDEFINED AS
		ATA17	→	FAST_RC
		ATA18	→	ALT_MUXPA20
		ENP92	= '1'	
	= 1	PORT92h functions, enabled, ENP92 = '1' (NOTE: Only MUXPA20 and FAST_RC are implemented. See Timing Diagrams (Figure 56 on the next page.))		
2	= 0	/CK8042 Pins (Frequency) = 7.14MHz (Nominal)		
	= 1	/CK8042 Pins (Frequency) = 11.5MHz (Nominal)		
3	= 0	16-bit I/O decode selected.		
	= 1	10-bit I/O decode selected.		
4,5,6,7	= 0	Reserved. Always program to '0'.		

Figure 8-26. INDEX48h, Mode Reconfigure

Note: The default '00h', initiated at system power-up, defines all pins to identical settings as those of Rev 'B' chips.

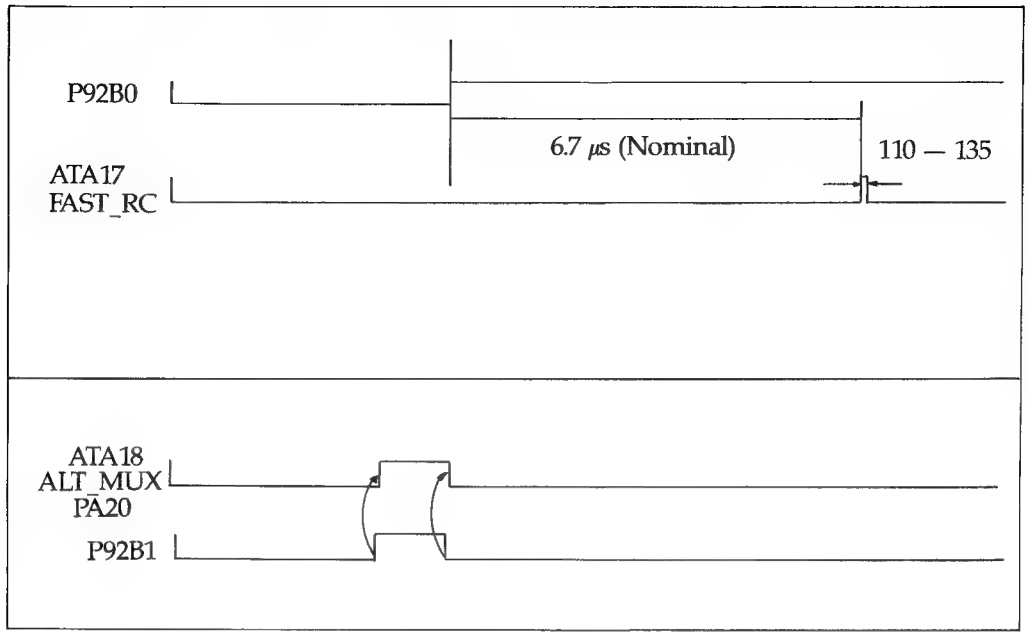


Figure 8-27. Port 92: FAST_RC and ALT_MUXPA20 Timing

On-board connections of FAST RC and MUXPA20

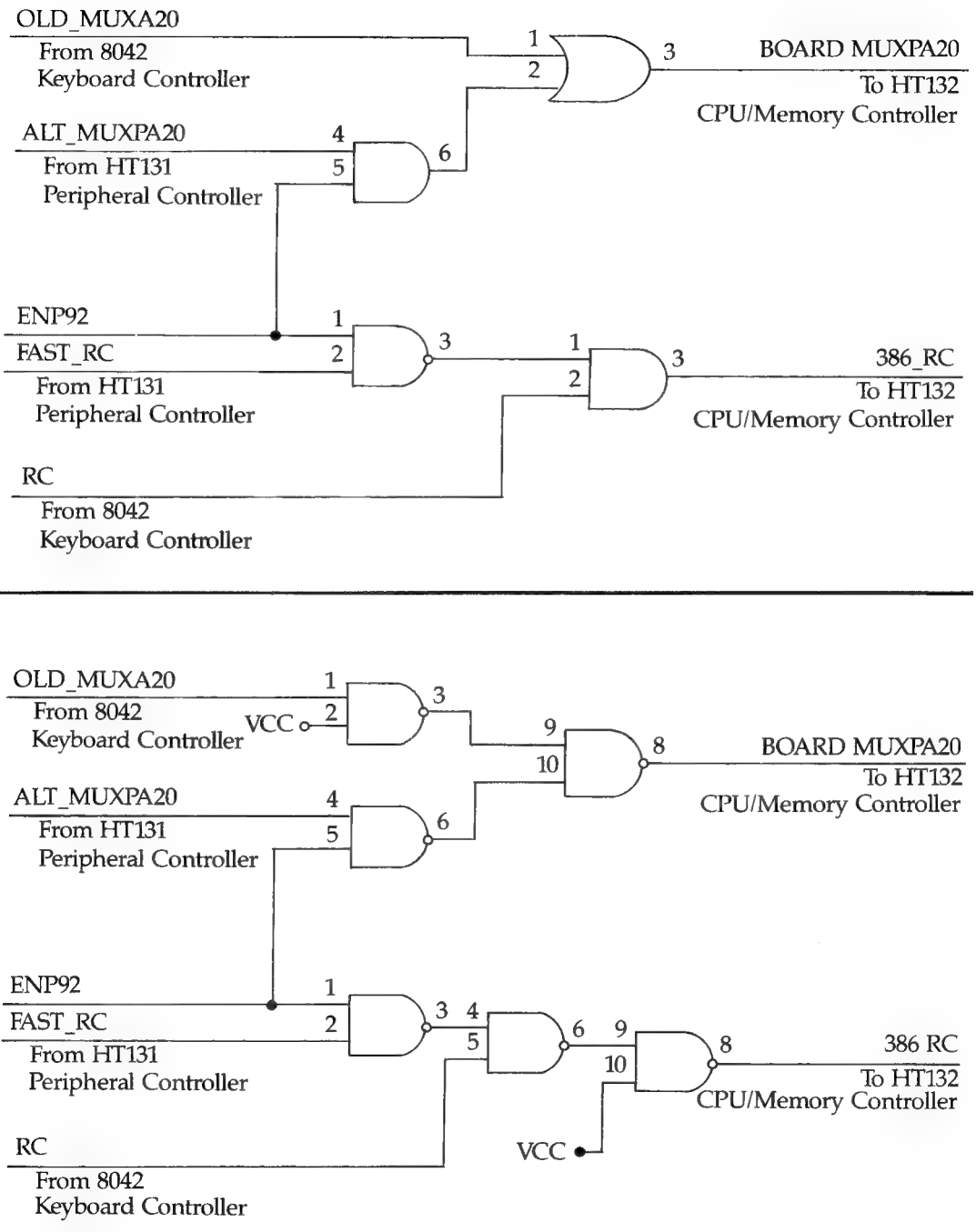


Figure 8-28. FAST_RC and ALT_MUXPA20 Connections

INDEX49h — Additional REFRESH Wait states

Default value = 00h
This register extends the range, in combination with the status of Bits 0..3 of INDEX42h, to 63 programmable REFRESH wait states. INDEX49h, as noted below, is available for the selection of REFRESH wait states in number greater than 15 — See INDEX42h for more information.

Bits	Value	Description
1,0		Additional REFRESH Wait States:
	0,0	Bits 1,0 = '0' represent up to 15 wait states available through INDEX42h.
	0,1	Represent 16 to 31 REFRESH Wait States available through INDEX42h.
	1,0	Represent 32 to 47 REFRESH Wait States available through INDEX42h.
	1,1	Represent 48 to 63 REFRESH Wait States available through INDEX42h.
7..2	0	Reserved. Always program to '0'.

Figure 8-29. INDEX49h, Additional REFRESH Wait States

PORT 92h —

Default value = 00h
This register is directly mapped into I/O location (PORT) 92h. Access to this register is enabled by programming INDEX48h Bit 1 to a value of '1'. Once enabled, this register (PORT92h) has the following definition.

Bit	**State**	**Meaning**
0	= 0	FAST_RC is selected OFF
	= 1	Apply FAST_RC (See Note*)
1	= 0	Set ALT_MUXPA20 (Pin) to the LOW condition.
	= 1	Set ALT_MUXPA20 (Pin) to the HIGH condition.
7-2	n/a	Reserved.

Figure 8-30. INDEX(Port)92h-FAST_RC and ALT_MUX PA20

Note: FAST_RC is a single 110-135ns positive pulse that occurs ~6.7μs after setting Bit 0 of PORT92h to a value of '1'. Bit 0 must be programmed back to a value of '0' before another FAST_RC pulse can be generated.

9

CACHE

9.1 DESCRIPTION

9.1.1. A38202 Microcache®

The Austek A38202 Microcache is a high-performance cache controller for Intel 80386 based systems. The Microcache provides high levels of integration and functionality. It interfaces directly to the 80386; no additional support logic is required. Because of its 80386-like bus interface, the A38202 can be added to existing 80386-based designs with a minimum of external logic.

The 80386, operating with the A38202 Microcache, runs with zero wait states in a cache read hit cycle. If the data is not present in the cache, it is fetched from main memory by the Microcache controller.

Table 9-1 summarizes the cache parameters which are implemented for the A38202.

Table 9-1. Microcache Parameters

Parameter	Value
Cache size	32, 64 or 128KB
Block size	64, 128 or 256 bytes
Subblock size	4 or 16 bytes
Number of groups	2
Number of tags	512

Cache Structure

The A38202 Microcache memory consists of four to sixteen (depending on cache configuration) static RAMS that contain the cache code and data. The A38202 has 18 kbits of static RAM on-chip (tag memory) which is used as a directory of presence information for the code and data being held in the cache memory.

Associativity

The A38202 Microcache implements a cache which may be direct mapped or 2-way set-associative. Set-associativity is a caching technique in which a number of possible locations exist in the cache memory for the block associated with any particular address. The number of locations is equal to the number of groups in the cache implementation. If there is only one group, the cache is direct mapped; if the number of groups equals the number of tags, the cache is fully associative. With the A38202, each location in main memory can reside in up to two possible locations in the cache.

Cache Coherency

The A38202 provides both software and hardware mechanisms to assure coherency of data in systems with other bus masters (such as other processors or DMA devices). The A38202 can purge any stale data by executing an invalidation instruction, or by monitoring the system bus for invalidation cycles (bus-watching).

Write Buffer Support

The A38202 Microcache on-chip system bus controller has full support for the use of a write buffer to increase system performance. The write buffer stores data output from the processor until the data can be written to main memory. The processor may continue operation without waiting for the main memory write to complete, thereby increasing processor performance.

9.1.2 A38202 Programming

The A38202 is capable of executing a set of instructions that manage the cache operating modes. These cache control instructions are issued as I/O instructions from the 80386, usually as part of the initialization process.

The A38202 may be programmed to perform the following control functions:

- Enable or disable the cache for normal operation
- Define the current cache configuration
- Define up to three independent memory regions as noncachable
- Enable or disable the noncachable memory regions
- Flush all of the cache contents
- Enable or disable cache RAM as local RAM

Creative use of the instruction set permits the system designer to achieve the full benefit of the A38202 Microcache capabilities.

9.1.3 A38202 Packaging

The A38202 Microcache is a 160,000 transistor VLSI device fabricated in 1.5 micron CMOS technology. The Microcache is available in a 160-lead EIAJ Plastic Quad Flat Pack (PQFP).

9.2 ARCHITECTURE

9.2.1 Internal Configuration

Circuitry on the A38202 Microcache comprises the following major functional units (as seen in figure 9-1).

1. Processor interface and control
2. Tag RAM groups
3. SRAM interface and control
4. System interface and control
5. Noncachable address comparators

Processor Interface/Control Unit

The control unit monitors the operation of the 80386, and keeps track of the current processor state. During read miss cycles, the control unit instructs the system interface unit to fetch the appropriate number of words from main memory.

Tag RAMS

The A38202 contains two tag RAM groups, each with 256 entries. Each entry consists of a tag and subblock presence information. The information stored in the tag RAMs identifies individual blocks that correspond to memory locations currently present in the cache memory. A set of high-speed comparators within each tag RAM responds to the current internal address bus values and indicates when requested data is present (signifying a cache read hit).

Static RAM Controller

The static RAM controller takes addresses from the internal address bus and performs read and write operations to the cache memory.

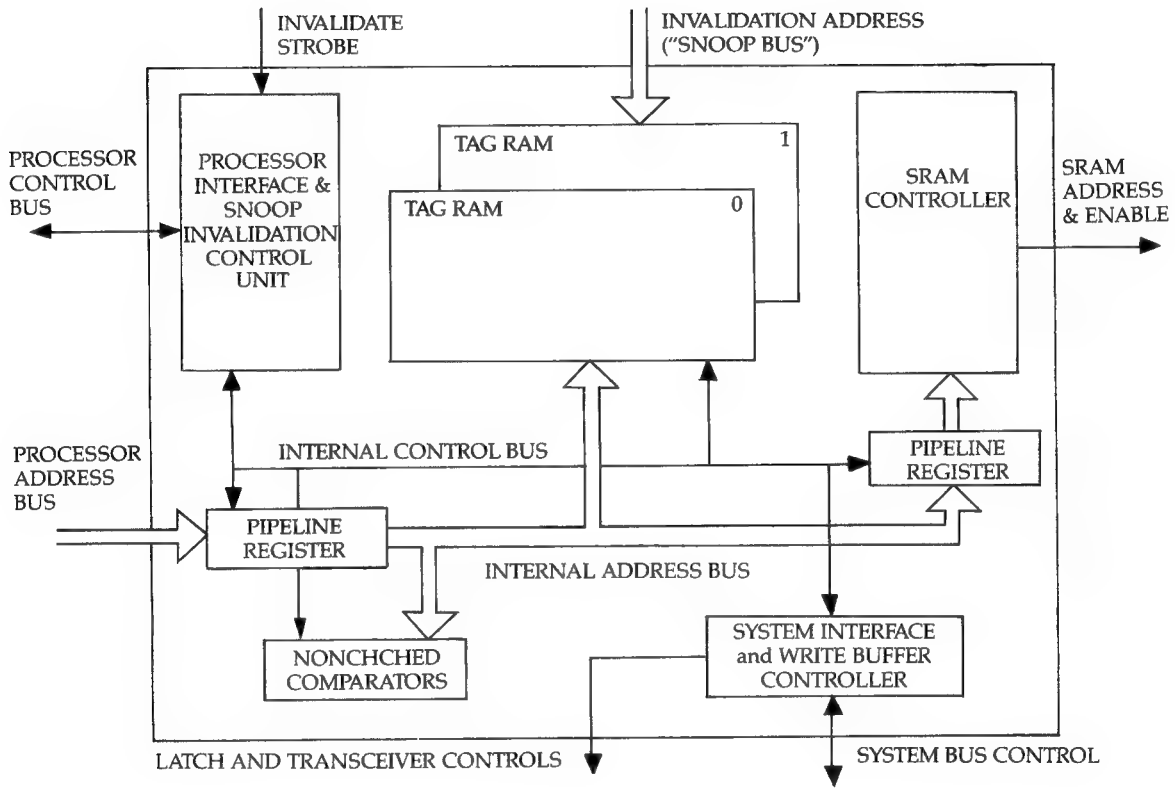


Figure 9-1. A38202 Internal Configuration

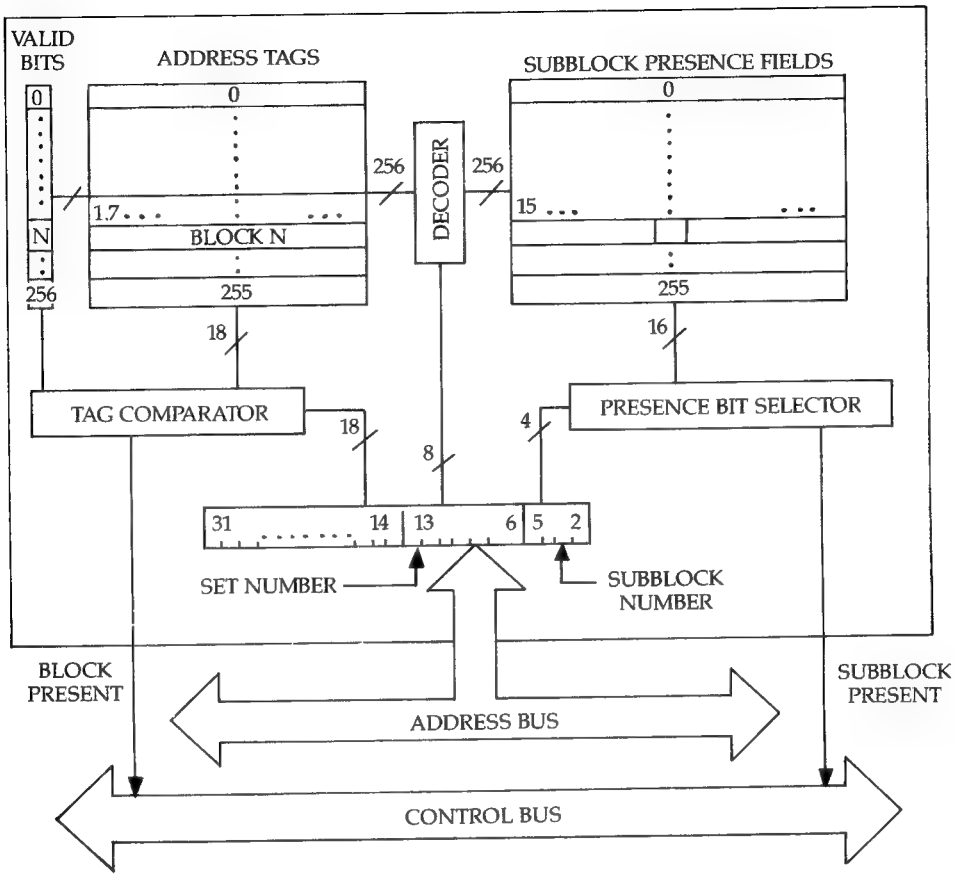


Figure 9-2. Tag RAM Organization

System Interface Controller

The system interface controller provides the handshaking and control signals to manage the system interface for any cycles which are not cache read hit cycles.

The system interface controller has been designed to resemble the 80386 bus interface, thus simplifying the design of the A38202 into existing 80386 systems.

Noncachable Address Comparators

Certain regions of main memory may be declared noncachable to avoid data conflicts that can arise out of some DMA operations or memory remapping carried out by an external device. These areas can be programmed into the A38202 by means of noncache descriptors. The noncached comparators continually monitor the internal address bus to detect accesses to memory locations that have been designated noncachable. The comparators signal the control unit when these accesses occur.

9.2.2 Cache Organization

The A38202 can be used to implement a number of varying cost/performance cache solutions. Cache size can be varied from 32kB to 128kB, and associativity can be direct mapped or 2-way set-associative.

There are 2 memory *groups,* each accessed in parallel during a bus cycle. Each group contains 256 entries consisting of a *tag* and cache data presence information (512 entries total). Each entry is associated with a *block* of data in the cache data memory. The block size varies from 64 bytes to 256 bytes as the cache size varies from 32kB to 128kB. The cache data memory is implemented in external high-speed RAM chips.

When the cache is accessed, an 8-bit field from the 32-bit physical address (called the *set number*) is used to access each group. Two tags are read and compared simultaneously to the tag field from the physical address. If there is no match (termed a *cache miss*), then the cache must fetch a block from system memory. Most system buses do not enable simple transfers of such a large number of bytes. Therefore the block is viewed as 8 or 16 (dependent on cache size) *subblocks* of 4 or 16 bytes each. Each entry in each group has a field which indicates the presence or absence of each individual subblock. Depending on the cache configuration, the A38202 fetches either 4 or 16 bytes from the system memory in one access.

The A38202 implements a *read-allocate* cache. For a read access, if the data is not present in the cache then a block is allocated in the cache for the data fetched from system memory. For a write access, if the data is not in the cache then it is only written to system memory-no space is allsocated in the cache for it.

9.2.3 Cache Coherency

Problems with cache coherency occur when another processor or bus controller writes data to a memory location which is stored in the cache. This leaves the cache with stale data, and the CPU may never be made aware of the new information.

The A38202 provides two mechanisms to solve the problem of cache coherency: a software mechanism that requires the operating system to manage the sharing of data and a hardware mechanism to indicate cycles which should be treated as invalidation requests.

Software Mechanisms for Coherency

The software solution to coherency requires that no two bus masters in a system share the same section of writable memory at any one time, with the exception of *locked* operations which always cause the cache to be transparent. The operating system must ensure that no two bus masters have concurrent access to a region of memory. When a region of memory is made available for access by the processor, its cache must be cleared of potentially stale entries for that region. Clearing this stale data can be performed by issuing an *invalidate-all* instruction to the cache controller.

For example, a DMA device in a multiprocessor system may be about to load a page of data from a disk after a request from the operating system. The operating system must ensure that no other bus master (MPU or DMA device) has concurrent access to the physical page. Once the transfer is complete, the processor must have any potentially stale data removed from its cache.

Hardware Mechanism for Coherency

The A38202 can also maintain coherency via *bus-watching* (also called *snooping*). The A38202 monitors system bus cycles, and when a write cycle by another bus master (such as a DMA controller) is detected, the address on the system bus is sampled. This address is then looked up in the cache directory, and if present, the entry associated with that address is invalidated. This will force the A38202 to fetch data from main memory the next time that address is accessed, ensuring that the 80386 gets the correct data from that address.

9.2.4 Noncachable Regions

The A38202 allows three separate areas of the 32-bit address space to be designated noncachable. Two of the regions are assignable on 64kB boundaries anywhere in the 4-GB physical address space of the 80386. The size of these region can range from 64kB up to 4GB. The third region is assignable on a 4kB boundary, and can range from 4kB up to 4GB. The regions may be separate, contiguous, or overlapping. These regions are suitable for ROM resident initialization routines, memory-mapped I/O devices, system control registers, dual port memory or any other memory that should not be cached.

9.3 A38202 SIGNALS

This section describes the A38202 Microcache input and output signals (refer to Figure 3-1). The signals are classified by the following functional groups:

Timing and processor signals
- Clock
- Reset
- Processor address
- Bus control
- Cycle definition

Status and control signals

Cache control signals
- Cache memory address
- Cache enables

System interface signals
- Cycle definition
- Bus control
- Chip select
- Write buffer control

Bus Watching signals
- Snoop Address
- Snoop Status

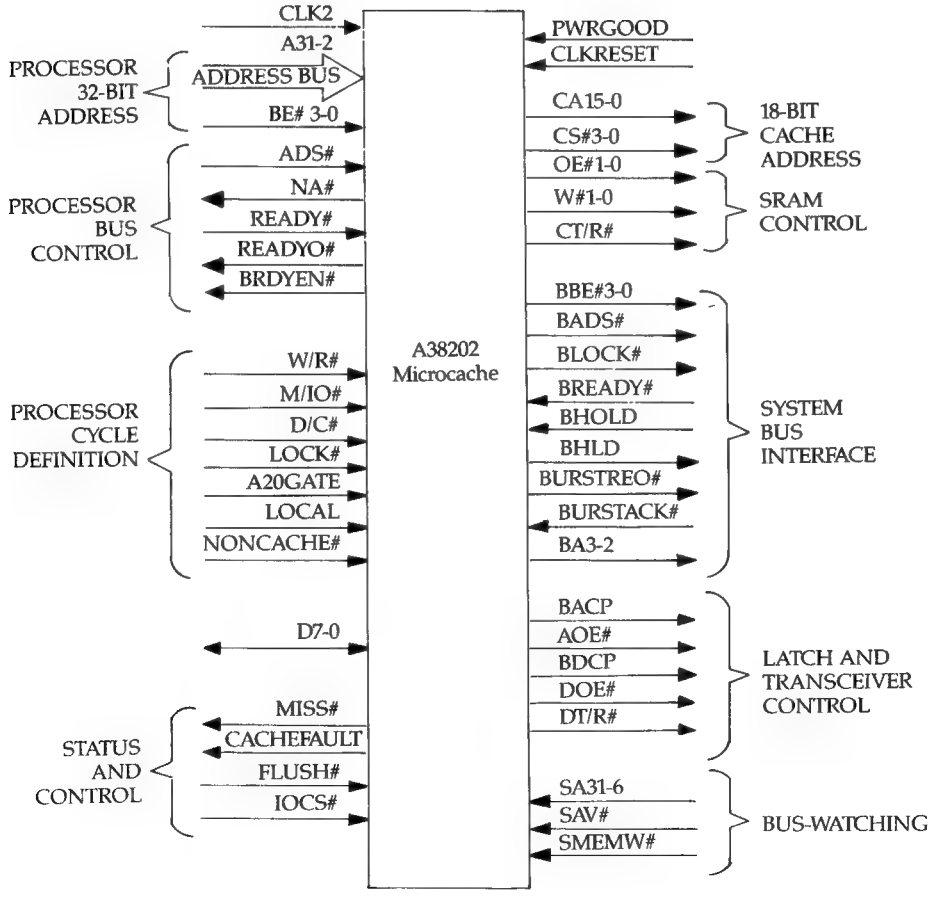


Figure 9-3. A38202 Signals

Signal Naming Conventions

The # symbol is used at the end of a signal name to indicate that the signal is asserted when it is at a low voltage level. The absence of the # at the end of the signal name indicates that the signal is asserted when it is at a high voltage level.

Example:

READYO# This signal is asserted when it is at a low voltage level.

CACHEFAULT This signal is asserted when it is at a high voltage level.

Individual signals from buses are indicated by appending the ordinal number of the signal in the bus to the name.

Example: A31 to A2.

9.3.1 Timing and Processor Signals

The timing and processor signals interface the A38202 Microcache to the 80386.

80386/A38202 Clock (CLK2)

CLK2 provides the fundamental timing for an 80386/A38202 system, and should be connected to the same source that drives the 80386 CLK2 input.

80386/A38202 Reset (CLKRESET, PWRGOOD)

The A38202 has two reset signals, PWRGOOD and CLKRESET. PWRGOOD should be sued as a power-on reset to the A38202. It sets the A38202 to a known state (see section 4.22 for details). CLKRESET is used by the A38202 to synchronize its internal clock. It should be connected to the RESET input of the 80386. This will ensure that the A38202 and 80386 are always in phase with each other.

Address Bus (A31-A2, BE3#-BE0#) and Cycle Definition Signals (M/IO#, D/C#, W/R#, LOCK#)

The A38202 connects directly to these outputs of the 80386. The address bus signals are used by the A38202 to perform its tag RAM lookup to determine whether the data the 80386 has requested resides in the cache. The cycle definition signals are decoded by the A38202 to determine the type of cycle the 80386 is executing.

Address Strobe (ADS#)

ADS# is asserted by the 80386 when new address and cycle definition signals are available. It is used to keep track of the state of the 80386.

Ready Input (READYI#)

READYI# is an input to the A38202 that indicates the completion of an 80386 bus cycle. It is used in conjunction with ADS# to keep track of the 80386 state. READYI# should be connected to the 80386s READY# input.

Next Address Request (NA#)

NA# is asserted by the A38202 to request the 80386 to enter pipelined mode.

Note: The A38202 must have exclusive control of the 80386's NA# signal.

Ready Output (READYO#) and Bus Ready Enable (BRDYEN#)

The A38202 directly terminates three types of cycles with its READYO# output. These are

- Cache Read Hit Cycles
- Posted Write Cycles
- I/O Accesses to the A38202

All other cycles are terminated by either devices on the 80386 local bus or the A38202's system bus. BRDYEN# is asserted by the A38202 during system bus cycles to gate BREADY# to the 80386.

Data Bus (D7-D0)

The data bus pins on the A38202 connect directly to the 80386. They are used to read/write the A38202s internal registers.

9.3.2 Other Cycle Definition Signals

A20 Gate (A20GATE)

This signal is used by the A38202 to determine whether it should use the value of A20 driven by the 80386 or force it to be low. This is required for compatibility with some 8088 and 8086 code. This input should be driven low when the 80386 is operating in real mode, and high when the 80386 is operating in protected mode.

Local Access (LOCAL)

This signal is used to tell the A38202 that the current bus cycle will be executed on the 80386s local bus. When it is asserted, the A38202 completely ignores the current cycle.

Noncachable Access (NONCACHE#)

This signal is used to tell the A38202 that the current bus cycle is an access to a noncachable region of memory. It allows external decoding of noncachable regions in addition to those defined by the internal noncachable region descriptors.

9.3.3 Cache Control Signals

These A38202 signals interface directly to the cache SRAMS.

Cache Address Bus (CA15-CA0)

The cache address bus connects from the A38202 to the external cache SRAMS. Note that some of these signals may not be used, depending on the size of the cache implemented.

Cache Output Enables (OE1#, OE0#)

OE0# and OE1# are active low signals which tie to the cache SRAM output enables. They respectively enable either bank 0 or bank 1 to drive the 80386 data bus. For direct mapped caches both of these signals are active (since there is only one bank of cache SRAM). For 2-way set-associative caches the state of these signals will reflect which set a match was found in.

Cache Write Enables (W1#, W0#)

W0# and W1# are active low signals which tie to the cache SRAM write enables. They respectively enable either bank 0 or bank 1 to write data from the 80386 data bus. For direct mapped caches both of these signals are active. For 2-way associative caches only one will be active, depending on which bank is to be updated.

Cache Chip Selects (CS3#-CS0#)

These active low signals connect to the cache SRAM chip selects and individually enable the four bytes of the 32-bit wide cache. During read hits, all four chip selects are enabled as the 80386 will ignore any data it does not require. All four chip selects are enabled during a cache read miss cycle so as to update the entire subblock. During write hit cycles, these signals reflect the state of the 80386s byte enable signals (BE3#-BE0#).

Cache Transmit/Receive (CT/R#)

This signal can be used to control optional data transceivers between the cache and the 80386 data bus. When high, the transceiver should be driving the 80386 local bus; when low, the transceiver should be driving the cache SRAM data inputs.

9.3.4 A38202 Local Bus Signals

The A38202 presents an 80386-like interface to the system. The signals discussed in this section are the A38202 equivalents of the 80386 signals.

Bus Address (BA3-BA2)

BA3-BA2 are the A38202 equivalent of the 80386s low two address bits. They are driven from the A38202 when multiple fetch cycles are required.

Bus Byte Enables (BBE3#-BBE0#)

BBE3#-BBE0# are the A38202 equivalent of the 80386 byte enables. These signals reflect the state of the 80386 byte enables, except during cache read miss cycles, when the A38202 drives all of them low. This ensures that a complete subblock is fetched to update the cache.

Bus Lock (BLOCK#)

BLOCK# is the A38202 equivalent of the 80386 LOCK# signal. When the 80386 executes a sequence of locked cycles, the A38202 executes the cycles on its local bus, regardless of whether the locations accessed currently reside in the cache. The A38202 will not allow another master to gain control of the bus while it is executing a sequence of locked cycles.

Bus Address Status (BADS#)

BADS# is the A38202 equivalent of the 80386 ADS# signal. When asserted, it indicates that a valid address and cycle definition signals are available.

Bus Ready Input (BREADY#)

A38202 local bus cycles are terminated by the assertion of BREADY#, just as 80386 cycles are terminated by READY#. BREADY# is also gated through to the 80386 by BRDYEN# to terminate its cycle.

Bus Arbitration Signals (BHOLD and BHLDA)

BHOLD is an input from another master requesting usage of the system bus. BHLDA is an output granting the bus to the requestor. The functionality is identical to that of the 80386s HOLD and HLDA signals.

9.3.5 Burst Mode Control Signals

When the A38202 is operating with 16-byte subblocks, four fetches are required to fill each subblock. In this case, the A38202 will request a burst fill by asserting BURSTREQ# at the start of the bus cycle.

If the system bus is able to respond with a burst of data, the signal BURSTACK# should be asserted during any BT2 T-state before the first assertion of BREADY#. If BURSTACK# is sampled asserted before BREADY#, th A38202 will expect to receive a burst of data to fill the subblock. If BURSTACK# is not simpled asserted before BREADY#, the A38202 will initiate three more read cycles to fill the subblock.

9.3.6 Latch and Transceiver Control Signals

The A38202 data bus is the system side of a latching transceiver, and the A38202 address bus is the system side of a latching buffer. The controls for these latches and transceivers are discussed in this section.

Latch Control Signals (BACK, AOE#)

These signals are designed to connect directly to an F or AS series 74374 or similar device. BACP is used to latch addresses from the 80386 on its rising edge. AOE# controls the output enable on the latches.

Transceiver Control Signals (BDCP, DOE# and DT/R#)

These signals are designed to connect directly to an F or AS series 74646 or similar device. BDCP is used to latch data on its rising edge. DOE# controls the output enable on the transceivers. DT/R# controls the direction of the transceivers. When DT/R# controls the direction of the transceivers. When DT/R# is high, the transceivers drive the system bus. When DT/R# is low, the transceivers drive the 80386 bus.

9.3.7 Status and Control Signals

Cache Miss Indication (MISS#)

On a cachable read miss cycle, this signal is asserted by the A38202. Its timing is the same as that of the other A38202 local bus cycle definition signals.

Cache Fault Indication (CACHEFAULT)

CACHEFAULT is asserted if the A38202 ever detects an internal error. After it is asserted, the A38202 will treat all accesses as if they were misses, regardless of the state of the cache directory. It can be cleared by resetting the cache (via PWRGOOD), executing an INVALIDATE ALL instruction or asserting the FLUSH# input.

Cache Flush (FLUSH#)

The FLUSH# input provides a hardware method for making the A38202 execute an INVALIDATE ALL instruction. After the directory has been cleared, all accesses will be misses until it fills up again.

I/O Chip Select (IOCS#)

This active low signal, when asserted, indicates to the A38202 that it has been selected in an I/O cycle. The A38202 will then load or store the currently selected internal register. See section 5.2 for more details.

9.3.8 Coherency Support Signals

These signals form the A38202s bus watching interface. The snoop bus connects to the system address bus if other bus masters exist at both the system and A38202 local bus level If masters exist only at the A38202 local bus level, these signals connect to the A38202 local address bus. In this case, SAV# should be connected to the nand of BM/IO#, BW/R# and BHLDA. SMEMW# should be connected to BADS#.

Note: These inputs may be asynchronous to CLK2.

Snoop Address Bus (SA31-SA6)

These signals are the inputs for the lookup and compare circuitry that determines when a snoop hit has occurred.

Snoop Bus Control (SAV#, SMEMW#)

SAV# and SMEMW# are the snoop bus equivalent signals to the A38202s local bus status signals. They are used to indicate to the A38202 when a valid cycle is present on th snoop bus. When SMEMW# is asserted and SAV# is low (indicating the snoop address is valid), the A38202 performs a snoop invalidation cycle.

9.4 PROGRAMMABLE REGISTERS AND INSTRUCTION SET

Programming the A38202 will generally be carried out by the operating system as part of the initialization process. Once the cache has been initialized, few instances will arise where additional programming is necessary.

The following instructions can be executed by the A38202 Microcache.

- INVALIDATE ALL: Invalidates all tags in the Microcache, effectively purging the cache of data.
- SET NONCACHED REGION DESCRIPTORS: Defines those memory addresses that are not be stored in the cache.
- ENABLE/DISABLE NONCACHED REGIONS: Turns on and off the noncached regions of memory.
- ENABLE/DISABLE CACHE: Enable/Disable caching of data from any address not declared as noncachable.
- ENABLE/DISABLE DIAGNOSTIC MODE: Enable the cache SRAM to be used as local RAM. Also puts the cache into a mode where the contents of the tag RAMs can be read out.
- SET CACHE OPERATING MODE: Sets the current operating mode (i.e. level of associativity, cache size etc.).

9.4.1 Programming Overview

The A38202 can execute a number of instructions. To program the A38202, it is accessed as an I/O device. When an I/O cycle occurs with the IOCS# input asserted, the A38202 assumes that the cycle is a register read or write cycle.

The A38202 takes up 8 locations in the 80386 I/O address space. These locations are on a quadword (8-bytes) boundary. However, only the first and fifth locations can actually be read or written within the 8 bytes. This is because the data lines on the A38202 connect to only the low 8 bits of the 80386s data bus. A2 is used to select between the high and low locations.

Registers within the A38202 are accessed by a register-indirect method. First, the address of the register to be read or written is written to the low I/O location assigned to the A38202 (i.e. IOCS# is asserted and A2 is low). Then the contents of that register can be read or written by performing the appropriate read or write I/O cycle to the high I/O location (i.e. IOCS# is asserted and A2 is high). Table 9-2 shows what value must be written to the address register to access each register within the A38202.

Table 9-2. A38202 Register Addresses

Address	Register
00H	Control Register
04H	Configuration Register
08H	Status Register
10H	Noncache Control Register
20H-22H	Noncache D0 Buttom Register (LSB to MSB)
24H-26H	Noncache D0 Top Register (LSB to MSB)
28H-29H	Noncache D1 Bottom Register (LSB to MSB)
2CH-2DH	Noncache D1 Top Register (LSB to MSB)
30H-31H	Noncache D2 Bottom Register (LSB to MSB)
34H-35H	Noncache D2 Top Register (LSB to MSB)

All other addresses are reserved to Austek, and should not be used. Writing to those addresses may cause unpredictable results.

Note: All bits in registers which are undefined are reserved to Austek and should always be written as 0.

9.4.2 Control Register

The control register shown in figure 9-4 determines the major operating modes of the A38202. The register contains 7 bits defined for control of operating modes.

I	P	IW	1367	BI/O	—	C	D

Figure 9-4. Control Register

The defined CONTROL REGISTER bits are described as follows:

D (Enable/disable diagnostic mode, bit 0)
If enabled (1), it forces the microcache to map the 32kB (to 128kB) of cache RAM into normal system memory address space beginning at address 40000H.

C (Enable/disable cache, bit 1)
If C is set to zero, the cache is disabled and all memory accesses are treated as noncachable. If C is set to one, then the cache is enabled.

BI/O (Buffer I/O Writes, bit 3)
The BI/O bit defines whether I/O write cycles should be buffered or not. If it is set, I/O writes are buffered.

I387 (Ignore 80387 cycles, bit 4)
When the I387 bit is set, the A38202 will ignore any 80387 cycles (i.e. I/O cycles with A31 high).

IW (Ignore Weitek cycles, bit 5)
When the IW bit is set, the A38202 will ignore any Weitek 1167/3167 cycles (i.e. cycles to memory addresses in the region C0000000H-C000FFFFH).

P (Pipelined mode, bit 6)
The P bit defines whether the A38202 should run the 80386 in pipelined mode. When set, the A38202 requires the 80386 to run in pipelined mode to perform zero wait-state read hits.

(Invalidate all, bit 7)
When the I is set to one all valid data in the cache is effectively purged by invalidating all tags in the cache.

Note that setting the D and C bits at the same time is meaningless; the C bit takes precedence and the effect is to enable caching.

9.4.3 Configuration Register

The CONFIGURATION REGISTER tells the A38202 what mode it is operating in. Figure 9-5 shows the details of the configuration register.

I/L	—	AS1	AS0	S16	—	CS1	CS0

Figure 9-5. Configuration Register

The defined CONFIGURATION REGISTER bits are described as follows:

CS1:0 (Cache Size, bits 0 & 1)
The two C bits define the cache size as described below.

00 32kB

01 64kB

10 128kB

11 Reserved to Austek

S16 (16-byte subblocks, bit 3)
When this bit is set, it forces the A38202 to use 16-byte subblocks, regardless of the cache size. Normally, the A38202 will only use 16-byte subblocks for 64kB and 128kB cache sizes.

AS1:0 (Cache Associativity, bits 4 & 5)
The A bits define the cache associativity as described below.

00 Direct Mapped

01 2-way

10 Reserved to Austek

11 Reserved to Austek

I/L (Interleaved/Linear DRAM, bit 7)
The I/L bit is used to change the order in which data is fetched during multiple fetch cycles (or the order in which data is expected during burst fills). This ordering is described in table 9-3.

Table 9-3. Multiple Fetch Data Ordering

Requested Address	Linear DRAM	Interleaved DRAM
0	1, 2, 3, 0	3, 2, 1, 0
1	2, 3, 0, 1	2, 3, 0, 1
2	3, 0, 1, 2	1, 0, 3, 2
3	0, 1, 2, 3	0, 1, 2, 3

9.4.4 Status Register

As shown in figure 9-6, the STATUS REGISTER contains 2 bits defined to indicate the current status of the A38202. This register is read only.

—	—	—	—	—	M	—	O

Figure 9-6. Status Register

The defined STATUS REGISTER bits are described as follows:

O (Invalidation Overflow, bit 0)
When set, indicates that invalidation requests occurred too frequently (i.e. more than once every two T-states) to be processed by the A38202.

M (Multiple Match, bit 2)
Indicates that a multiple match error occurred in the tag RAMS.

9.4.5 Noncache Registers

Noncache Control Register

This register contains 6 bits, which control the enabling of each noncache descriptor for read or write access. Note that setting a read enable bit forces the corresponding write enable bit to be set. The format of the register is shown in figure 9-6.

—	W2	W1	W0	—	R2	R1	R0

Figure 9-7. Noncache Control Register

The defined NONCACHE CONTROL REGISTER are as follows:

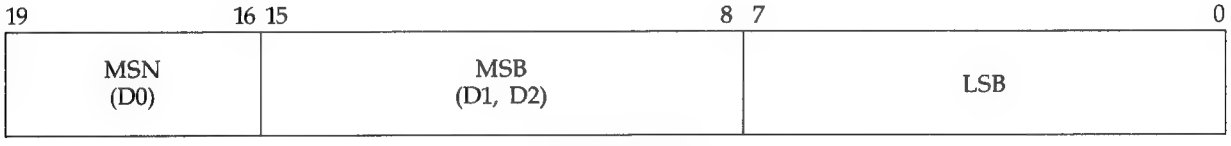
R2:0 (Read Enables, bits 2:0)
These bits enable their corresponding noncache region descriptor for read accesses. When one of these bits is set, it forces the corresponding write enable to be set as well.

W2:0 (Write Enables, bits 6:4)
These bits enable their corresponding noncache region descriptor for write accesses.

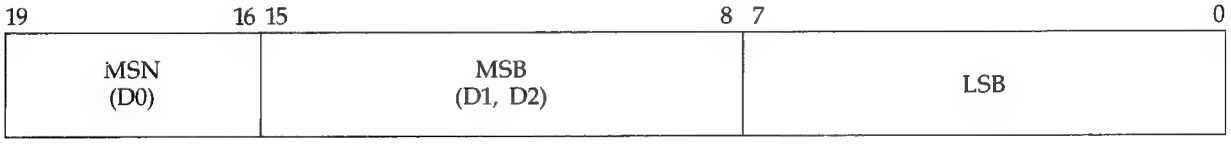
Noncache Region Descriptors

There are three descriptors, D0, D1 and D2, enabled by the corresponding bits in the noncache control register. The noncache descriptors consist of two registers, a "bottom" register and a "top" register (see figure 9-7). These two registers define a region of addresses which is compared against the most significant bits of physical address. For descriptors D1 and D2, these registers are 16 bits wide, allowing the region to be positioned on any 64kB boundary. Descriptor DOS registers are 20 bits wide, allowing the region to be positioned on any 4kB boundary.

The "bottom" register defines the lowest address which is to be made noncachable. The "top" register defines the highest address which is to be made noncachable. The processor address is compared against the contents of the two registers, and any address which satisifies "bottom" ← address ← "top" is considered to be noncachable. Thus setting the contents of the "top" register to be less than that of the "bottom" register effectively disables a descriptor.



Bottom Register



Top Register

Figure 9-8. Noncache Descriptor Registers

To program the Noncache descriptors, use the LOAD NONCACHE DESCRIPTOR instructions. These instructions allow the processor to change the base addresses and lengths of the noncache spaces by loading data into the registers a byte at a time.

Note: When loading the Noncache Descriptors, caching should be temporarily disabled by clearing the C bit in the control register. After the descriptors have been changed, caching should be reenabled and an INVALIDATE ALL instruction should be issued to ensure that no cache coherency problems occur.

9.4.6 Initial Values

When the PWRGOOD input to the A38202 is asserted, the internal registers have the values shown in Table 9-4. The initial value of the CONTROL REGISTER, 30H, tells the A38202 to ignore 80387 and Weitek cycles, not to buffer I/O writes, and to run in non-pipelined mode. The initial value of the configuration register, 11H, defines the caching mode to be a 2-way set-associative 64kB cache. The initial value of the noncache descriptors are set up to make 256kB from C0000H to FFFFFH of the 80386s address space noncachable (descriptor D0), 128kB from A0000H to BFFFFH (descriptor D1), and 128kB from 80000H to 9FFFFH (descriptor D2). Only descriptor D1 is enabled (the initial value of the NONCACHE CONTROL REGISTER is 22H).

Table 9-4. Register Values after Reset

Control Register	30H
Configuration Register	11H
Status Register	00H
Noncache Control Register	22H
Descriptor D0 Bottom Register	000C0H
Descriptor D0 Top Register	000FFH
Descriptor D1 Bottom Register	000AH
Descriptor D1 Top Register	000BH
Descriptor D2 Bottom Register	0008H
Descriptor D2 Top Register	0009H

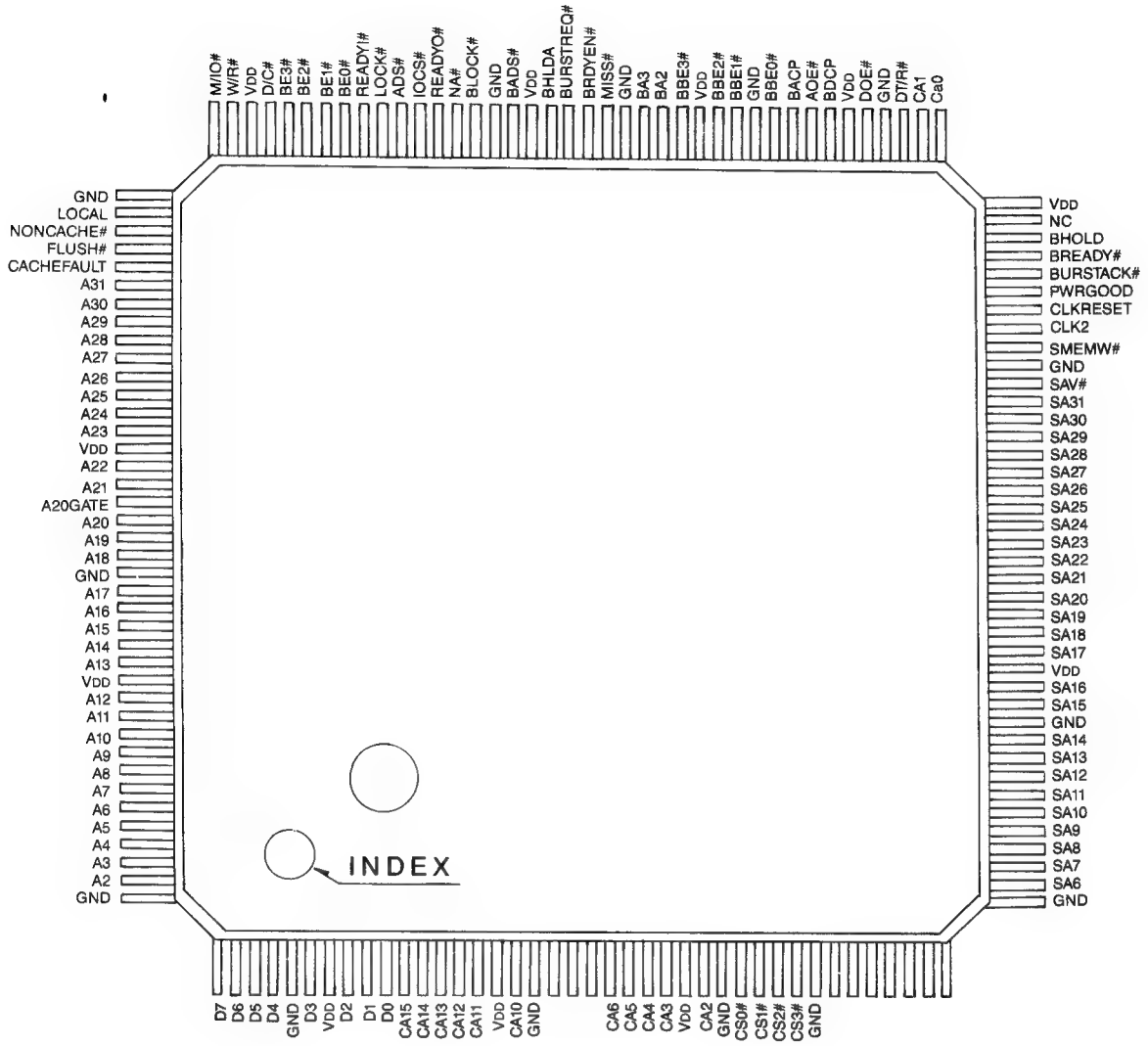


Figure 9-9. PQFP Pinout

10

1287 REAL-TIME CLOCK (RTC)

10.1 INTRODUCTION

The system board uses a 1287 real-time clock (RTC) module for its real-time clock and configuration memory. The RTC module combines a complete time-of-day clock with alarm, 100-year calendar, a programmable periodic interrupt, 50 bytes of low power user static random access memory (SRAM), and battery. System provisions allow the RTC to operate in a low power mode and protect the contents of both the RAM and clock during system power up and power down. The battery maintains clock and calendar information in RAM. The system does not charge the battery. If the battery fails, the 1287 must be replaced. Figure 10-1 illustrates the RTC memory map. An additional 14 bytes of CMOS RAM is used for the internal clock circuitry.

10.2 RTC RAM I/O OPERATIONS

The RTC sets the system time and data. The RTC updates at one-second intervals and automatically adjusts at the end of months and leap years.

Writing the correspondig index address to I/O port 70H allow reading and writing of the 64 locations in the RTC. The RTC address register latches the address and points to the specified byte in the RTC.

Values can be written to or real from all 64 bytes except for the following which are read only:

- Status registers C and D
- High-order bit (bit 7) of status register A
- High-order bit (bit 7) of the seconds byte

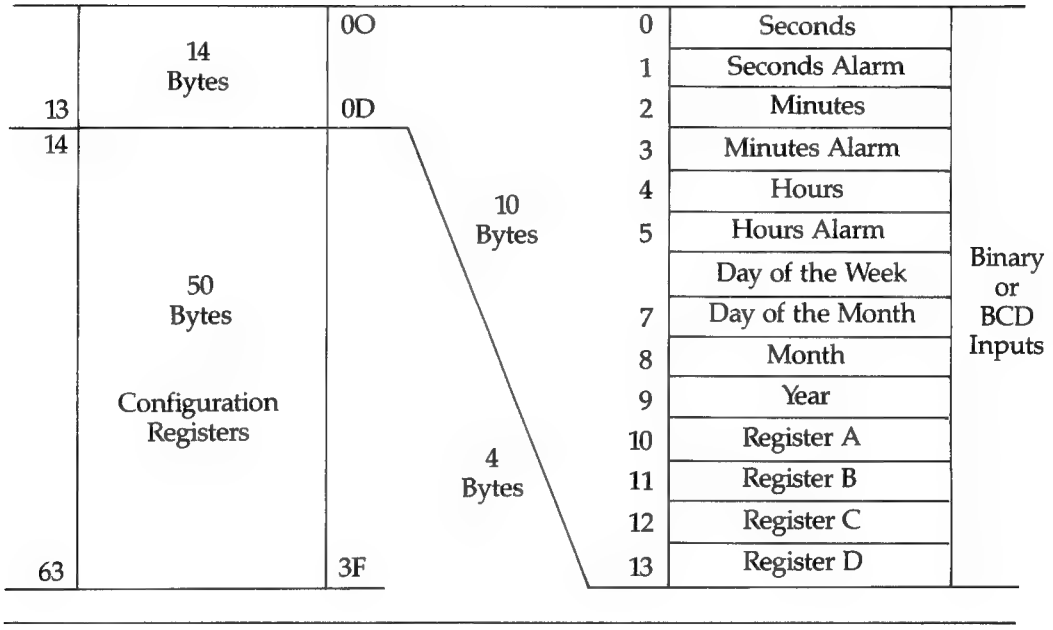


Figure 10-1. RTC Memory Map

Perform the following two steps when writing data into the RTC/RAM:

1. Write the RAM address (data = 00H through 3HF) into I/O port address 70H.

2. Write the data byte into I/O port 71H.

Perform the following two steps when reading data from the RTC/RAM.

1. Write the RAM address (data = 00H through 3FH) into I/O port address 70H.

2. Read the data byte from I/O port 71H.

Note: I/O port address 70H is also an output port for the NMI mask. Data bus bit 7 connects to the NMI mask bit and bits 0 through 5 connect to the RTC/RAM address lines.

During normal operation, the RTC performs an update cycle once every second. Divider bits DV2:0 and the SET bit in register B determine the performance of an update cycle. Divider bits DV2:0 must not be cleared and the register B set bit must be cleared. During an update, the lower 10 registers are no available to the CPU. The update cycle increments the clock/calendar registers and compares them to the alarm registers. An interrupt is issued if a match occurs between the two sets of registers (with enabled allarm and interrupt control bits).

10.3 RTC INTERNAL ADDRESSABLE LOCATIONS

The 64 addressable locations in the RTC are divided into 10 bytes containing the time, calendar, alarm data, four control and status bytes, and 50 general purpose RAM bytes (refer to Table 10-1). Table 10-1 also details the internal register/RAM organization of the RTC.

Table 10-1. Real-time Clock Address Map

Function	Index
Seconds	00H
Seconds alarm	01H
Minutes	02H
Minutes alarm	03H
Hours	04H
Hours alarm	05H
Day of week	06H
Date of month	07H
Month	08H
Year	09H
Status register A	0AH
Status register B	0BH
Status register C	0CH
Status register D	0DH
Diagnostic status byte	0EH
Shutdown status byte	0FH
Floppy disk drive type bypte	10H
Reserved	11H
Fixed disk type byte	12H
Reserved	13H
Equipment byte	14H

(continued)

Table 10-1. Real-time Clock Address Map *(continued)*

Function	Index
Low base memory byte	15H
High base memory byte	16H
Low expansion memory byte	17H
High expansion memory byte	18H
Drive C extended type byte	19H
Drive D extended type byte	1AH
Reserved	1BH
Reserved	1CH
Reserved	1DH
Reserved	1EH
Features installed: reserved	1FH
Drive type 48 parameters	20H-27H
Options 1	28H
Reserved	29H
Reserved	2AH
Options 2	2BH
Options 3	2CH
Reserved	2DH
2-byte CMOS RAM checksum	2EH-2FH
Low expansion memory byte	30H
High expansion memory byte	31H
Date century byte	32H
Setup information	33H
CPU speed	34H
Drive type 49 parameters	35H-3CH
Reserved	3DH-3FH

10.3.1 Time, Calendar, and Alarm Bytes

The CPU obtains time and calendar information by reading the appropriate locations in the RTC. Writing to these locations initializes the time, calendar, and alarm information. Information stored in these locations is in binary coded decimal (BCD) format.

Before initializing the internal registers, the set bit in register B must be set to 1 to prevent RTC updates. Once set, the CU initializes the first 10 locations in BCD format and the set bit is cleared.

Once initialized and enabled, the RTC performs clock/calendar updates at a 1Hz rate. During updates, the 10 bytes of time, calendar, and alarm information are not available for reading or writing by the CPU for 2 ms.

Table 10-2 lists the format for the 10 clock, calendar, and alarm locations. System software sets the RTC to BCD data mode.

Table 10-2. Time, Calendar, and Alarm Data Format

Function	Index	BCD Data
Seconds	00	00:59
Seconds alarm	01	00:59
Minutes	02	00:59
Minute alarm	03	00:59
Hours	04	
(12 hour mode)		01:12 (AM)
(24 hour mode)		00:23
Hours alarm	05	
(12 hour mode)		01:12 (AM)
(24 hour mode)		00:23
Day of week	06	01:07
Date of month	07	01:31
Month	08	01:12
Year	09	00:99

Note: The RTC does not affect the 50 bytes of RAM from index address 0EH to 3FH. These bytes are accessible during the update cycle.

10.4 STATUS REGISTERS

The four control and status bytes (status registers A:D) control the operation and monitor the status of the RTC. These registers, located at index addresses 0A:0DH, are accessible by the CPU at all times (refer to Tables 10-3 through 10-6).

Note: A setup program must initialize status registers A through D when setting the time and date.

10.4.1 Status Register A (0AH)

Table 10-3. Status Register A (0AH)

Bit	Function
7	Update in progress (UIP) bit 1 = The time update cycle in progress 0 = The current date and time accessed
6:4	Divider selection (DV2:0) bits These bits control the divider/prescaler on the RTC. They specify the time-base frequency (in KHz) used. The system initializes to 010, specifying a time base of 32.768KHz.
3:0	Rate selection (RS3:0) bits These bits select the divider output frequency. The system initializes to 0110, which selects a 1024Hz divider frequency and an interrupt rate of 976.562μs.

10.4.4 Status Register D (0DH)

Table 10-4. Status Register B (0BH)

Bit	Function
7	Set update cycle (SET) bit 1 = Abort the update cycle in progress Set to 1 for system initialization. 0 = Enable normal update cycle of one count per second.
6	Periodic interrupt enable (PIE) bit. This read/write bit selects an interrupt occurring at a rate specified by the rate and divider selection bits in register A. 1 = Enable the generation of periodic interrupts 0 = Disable the interrupt (default)
5	Alarm interrupt enable (AIE) bit. 1 = Enable the alarm interrupt 0 = Disable the alarm interrupt (default)

(continued)

Table 10-4. Status Register B (0BH) *(continued)*

Bit	Function
4	Update-ended interrupt enable (UIE) bit. 1 = Enable the update-ended interrupt. 0 = Disable the update-ended interrupt (default)
3	Sequare wave enable (SQWE) bit 1 = Enable the square-wave frequency set by the rate selection bits in register A. 0 = Disable square-wave frequency (default)
2	Date mode (DM) bit. Indicates whether the time and data calendar updates use binary or the BCD format. 1 = Select binary format. 0 = Select BCD format (default)
1	24/12-hour (24/12) bit. Determines whether 24-hour mode or 12-hour mode is set in the hours byte. 1 = 24-hour mode (default) 0 = 12-hour mode
0	Daylight savings enabled (DSE) bit. 1 = Daylight savings time enabled. 0 = Daylight savings time disabled (default).

10.4.3 Status Register C (0CH)

Table 10-5. Status Register C (0CH)

Bit	Function
7	IRQF (interrupt request flag) Set to 1 when any of the conditions cause an interrupt is true and the interrupt enable for that condition is true.
6	PF (periodic interrupt flag). Set to 1 when a transition, selected by RS3:0, occurs in the divider chain. This bit becomes active, independent of the condition of the PIE control bit. The PF bit generates an interrupt and sets IRQF if PIE = 1.
5	AF (alarm interrupt flag). Set to 1 when a match occurs between the time registers and alarm registers during an update cycle. The flag is independent of the condition of the AIE, and generates an interrupt it AIE is true.
4	UP (update ended interrupt flag). Set to 1 when an update ends. This flag is also independent of the condition of the UIE, and generates an interrupt it UIE is true.
3:0	Reserved

10.4.4 Status REgister D (0DH)

Table 10-6. Status Register D (0DH)

Bit	Function
7	Valid RAM and time (VRT) bit. This read-only bit determines the condition of the RTC internal battery. 1 = Battery operational. 0 = A low power sense. Indicates a dead battery in the RTC.
6:0	Reserved

10.5 CONFIGURATION BYTES

The configuration bytes provide information on diagnostic status, shutdown status, equipment, memory and other configuration parameters (refer to Table 10-7 through 10-24).

10.5.1 Diagnostic Status Byte (0EH)

Table 10-7. Diagnostic Status Byte (0EH)

Bit	Function
7	RTC chip battery power status. 1 = Power off 0 = Power on
6	Configuration record (checksum status indicator). 1 = Checksum not valid 0 = Checksum valid
5	Incorrect configuration information. Checks the equipment byte of the configuration record when the system powers up. 1 = Configuration information not valid 0 = Configuration information valid
4	Memory size comparison. 1 = Memory size different from configuration record 0 = Memory size the same as configuration record
3	Initial state of drive C or fixed disk drive controller. 1 = Wrong controller or drive C. System cannot boot from drive C. 0 = Correct controller and drive. The system boots from drive C.
2	Time status indicator (post checks) 1 = Time not valid 0 = Time valid
1:0	Reserved

Note: In order for the configuration information to be valid, power-on check requires at least one floppy disk drive installed (bit 0 of the equipment byte set to 1) and the display switch setting matches with the display controller installed.

10.5.2 Shutdown Status Byte (0FH)

When the CPU resets, the shutdown status byte is set.
The reset code identifies the type of reset and signals the system what to do after the reset. It also provides a method of resetting the system without losing previously stored data or returning the system to the real mode from protected mode.

Table 10-8. Shutdown Status Byte (0FH)

Bit	Function
7	Reset information. 00H = Normal system reset 09H = User software reset (return from protected mode) 01H:08H = Used by hardware self-test 0AH:FFH = Used by hardware self-test

10.5.3 Floppy Disk Drive Type Byte (10H)

Table 10-9. Floppy Disk Drive Type Byte (10H)

Bit	Function
7:4	First floppy disk drive type 0000 = No floppy disk drive 0001 = 360K drive (5.25-inch) 0010 = 1.2M high-density drive (5.25-inch) 0011 = 720K (3.5-inch drive) 0100 = 1.4M (3.5-inch drive) 0101:1111 = Reserved
3:0	Second floppy disk drive type 0000 = No floppy disk drive 0001 = 360K drive (5.25-inch) 0010 = 1.2M high-density drive (5.25-inch) 0011 = 720K (3.55-inch drive) 0100 = 1.4M (3.5-inch drive) 0101:1111 = Reserved

10.5.4 Fixed Disk Type Byte (12H)

Table 10-10. Fixed Disk Type Byte (12H)

Bit	Function
7:4	First fixed disk drive type (drive C) 0000 = No fixed disk drive installed 0001:1110 = Types 1-14 1111 = Types 16-255 (refer to extended byte 19H)
3:0	Second fixed disk drive type (drive D) 0000 = No fixed disk drive installed 0001:1110 = Types 1-14 1111 = Types 16-255 (refer to extended byte 1AH)

10.5.5 Equipment Byte (14H)

The hard ware self-test uses the equipment byte.
The format of the equipment byte is described in Table 10-11.

Table 10-11. Equipment Byte (14H)

Bit	Function
7:6	Number of floppy disk drives installed 00 = 1 drive 01 = 2 drives 10 = Reserved 11 = Reserved
5:4	Type of video display controller used 00 = Extended functionality controller 01 = Color graphic video display controller in 40-column mode 10 = Color graphic video display controller in 80-column mode 11 = Monochrome display controller
3:2	Not used
1	Presence of a numeric coprocessor 1 = Numeric coprocessor installed 0 = No numeric coprocessor
0	Presence of floppy disk drive 1 = Floppy disk drive installed 0 = No floppy disk drive

10.5.6 Low and High Base Memory Bytes (15H and 16H)

Table 10-12. Low and High Base Memory Bytes (15H and 16H)

Bit	Function
7:0	Address 15H (low-byte base size)
7:0	Address 16H (high-byte base size) 0100H = 256K RAM 0200H = 512K RAM 0280H = 640K RAM

10.5.7 Requested Low and High Memory Expansion Bytes (17 and 18)

This word indicates the total amount of expansion memory (above 1M) set by the system configuration program.

Table 10-13. Low and High Memory Expansion Bytes (17H and 18H)

Bit	Function
7:0	Address 17H (low-byte expansion size)
7:0	Address 18H (high-byte expansion size) 0200H = 512K RAM expansion 0400H = 1024K RAM expansion 0600H = 1536K RAM expansion 3C00H = 15360K RAM expansion

10.5.8 Drive C Extended Byte (19H)

Table 10-14. Drive C Extended Byte (19H)

Bit	Function
7:0	Addresses 00H:0FH (reserved) Addresses 10H:FFH (types 16:255)

10.5.9 Drive D Extended Byte (1AH)

Table 10-15. Drive D Extended Byte (1AH)

Bit	Function
7:0	Addresses 00H:0FH (reserved) Addresses 10H:FFH (types 16:255)

10.5.10 Feature Installed Byte (1FH)

Table 10-16. Feature Installed Byte (1FH)

Bit	Function
7:3	Reserved
2	Floppy disk drive A installed
1	Video display installed
0	Keyboard BIOS installed

10.5.11 CMOS RAM Checksum (2EH and 2FH)

The CMOS RAM checksum is the sum of the values from addresses 10H through 2DH.

Table 10-17. CMOS RAM Checksum (2EH and 2FH)

Bit	Function
7:0	Address 2EH (high byte of checksum)
7:0	Address 2FH (low byte of checksum)

10.5.12 FXD Type 48 Parameters (20H-27H)

Table 10-18. FXD Type 48 Parameters (20H-27H)

Bit	Function
20H	Cylinder low byte
21H	Cylinder high byte
22H	Number of heads
23H	Write pre-compensation start cylinder low byte
24H	Write pre-compensation start cylinder high byte
25H	Landing zone cylinder low byte
26H	Landing zone cylinder high byte
27H	Sectors per track

10.5.13 Shadow and Enter Setup (28H)

Table 10-19. Shadow and Enter Setup (28H)

Bit	Function
7	Cache disable
6	ROM BIOS map address 1M and 16M
5	Speaker off
4	512-640K enable
3	Enter Setup program at pre-boot only
2	AT32 I/O enabled
1	Video shadow disabled
0	System BIOS shadow disabled

Note: Video BIOS, alone, cannot be shadowed. It must be shadowed with the system BIOS.

10.5.14 Actual Low and High Extended Memory Bytes (30H and 31H)

The low and high extended memory bytes represent the total extended memory (above 1M) determined during system power up. System interrupt 15H determnes extended memory size.

Table 10-20. Low and High Extended Memory Bytes (30H and 31H)

Bit	Function
7:0	Address 30H (low-byte extended memory size) Address 31H (high-byte extended memory size) 0200H = 512K RAM exttended 0400H = 1024K RAM extended 0600H = 1536K RAM extended 3C00H = 15360K RAM extended

10.5.15 Date Century Byte (32H)

The date century byte is the century part of the current date encoded in BCD format.

Table 10-21. Date Century Byte (32H)

Bit	Function
7:0	BCD value for century (BIOS sets and reads this value)

10.5.16 Setup Information (33H)

Table 10-22. Setup Information (33H)

Bit	Function
7	128K ROM expansion or 512-640K
6	Enable user message after initial setup
5	Reserved
4	Copy of the 386 CR0 ET bit (will always be 1, regardless if a 387 is present or not)
3:0	Reserved

10.5.17 CPU Speed (34H)

Table 10-23. CPU Speed (34H)

Bit	Function
7:3	Reserved
2:0	CPU speed

10.5.18 FXD Type 49 Parameters (35H-3CH)

Table 10-24. FXD Type 49 Parameters (35H-3CH)

Bit	Function
20H	Cylinder low byte
35H	Cylinder low byte
36	Cylinder high byte
37H	Number of heads
38H	Write pre-compensation start cylinder low byte
39H	Write pre-compensation start cylinder high byte
3AH	Landing zone cylinder low byte
3BH	Landing zone cylinder high byte
3CH	Sectors per track

11

COMMUNICATION PORTS

11.1 INTRODUCTION

The chapter provides reference data for two RS-232C serial communication ports and one parallel printer port on the system board. Included are all addresses and interrupt levels.

11.2 SERIAL COMMUNICATION PORTS

Two 82510 asynchronous serial controllers provide interfacing between the communication ports and the CPU. Refer to Table 11-1 for selection of port addresses and interrupt levels.

Table 11-1. Selection of Addresses and Interrupt Levels

Port	Designation	Address	Interrupt
1	COM1	3F8-3FFH	IRQ4
2	COM2	2F8-2FFH	IRQ3

11.2.1 CPU Interfacing

Two 82510 controllers provide the interfacing between the communication ports and the CPU. The 82510 is a demultiplexed bus interface using a bidirectional, buffered, 8-bit data bus and a 3-bit address bus. Thirty-five registers, divided into four banks, control and configure the 82510 controllers.

11.2.2 Connectors and Pinouts

System board header J13B provides signals for both ports and connects to two DB9 RS-232 connectors (COM1 and COM2). Refer to Chapter 18 for pinout information of the serial communication connectors.

11.3 PARALLEL PRINTER PORT

The system board uses one parallel printer port. The parallel printer port provides a one way interface to a printer. Onboard jumpers select the leading or trailing edge of printer acknowledge and enables interrupt generation. Discrete logic provides interfacing between the parallel printer port and the printer. Setting jumper on the system board selects the port addresses and interrupt levels (refer to Table 11-2).

Table 11-2. Port Address and Interrupt Levels

Port	Address	Interrupt
LPT1	0378:037FH	IRQ7
LPT2	0278:027FH	IRQ5

11.3.1 Programming

The system board uses the read, write, status, and control signal registers to transmit data and status to and from the printer. System software executes all printer controls. Tables 11-3 and 11-4 list input and output instruction information. Table 11-5 lists the parallel port registers.

Table 11-3. Input Instructions

Input Instruction	Port 1	Port 2
Data Read	0378H	0278H
Status Read	0379H	0279H
Control Signal Read	037AH	027AH

Table 11-4. Output Instructions

Output Instruction	Port 1	Port 2	Function
Write Data	0378H	0278H	Character to Print
Write Control	037AH	027AH	STROBE
			INITIALIZE
			AUTO FEED
			SLCTIN Enable int

Table 11-5. Parallel Port Registers (Bits 7-4)

REGISTER	BIT7	BIT6	BIT5	BIT4
Read Port	PD7	PD6	PD5	PD4
Read Status	BUSY	ACK	PE	SELECT
Read Control	1	1	1	IRQ ENB
Write Port	PD7	PD6	PD5	PD4
Write Control	1	1	1	IRQ ENB

Table 11-6. Parallel Port Registers (Bits 3-0)

REGISTER	BIT7	BIT6	BIT5	BIT4
Read Port	PD3	PD2	PD1	PD0
Read Status	ERROR	1	1	1
Read Control	SELECT	INT	AUTOFEED	STROBE
Write Port	PD3	PD2	PD1	PD0
WRITE Control	SELECT	INT	AUTOFEED	STROBE

11.3.2 Connector and Pinouts

J13A is a 2×13 (26-pin) header connected to a DB25 connector. Refer to Chapter 18 for pinout information on the parallel printer connector.

12

KEYBOARD AND MOUSE CONTROLLER

12.1 INTRODUCTION

The system board supports a 101- or 102-key enhanced keyboard and a three button mouse. An Intel 8742 microcontroller controls the keyboard and mouse system interface (see Figure 12-1). This chapter describes the keyboard and mouse interface through the 8742 microcontroller.

12.2 KEYBOARD AND MOUSE CONTROLLER SYSTEM INTERFACE

The keyboard and mouse controller communicates with the system through an 8-bit read-only status register at I/O address 64H, a read only output buffer at I/O address 60H, and an input buffer. The input buffer consists of two parts: a data byte and a command byte written at addresses 60H and 64H, respectively.

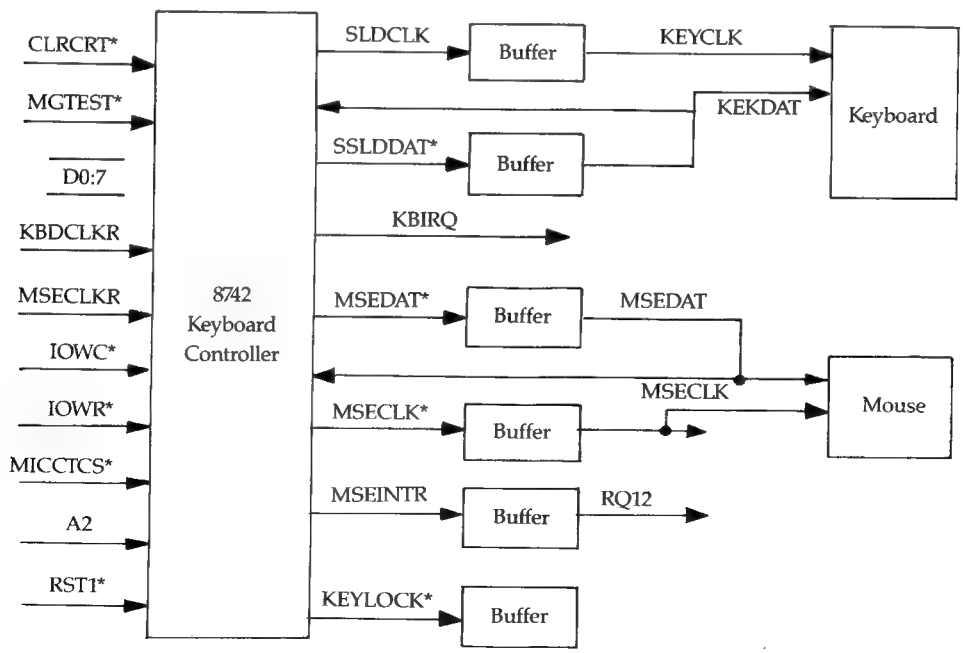


Figure 12-1. Keyboard/Mouse Controller

12.2.1 Status Register

The controller status register contains information about the state of the controller and system interface (refer to Table 12-1).

Table 12-1. Status Register Bit Definition

Bit	Function
0	Output buffer (I/O Address 60H) full. 0 = No data from the keyboard in the output buffer (DBBOUT) 1 = The keyboard controller loaded the output buffer with data. This bit is set to 0 when the CPU reads it (DBBIN).
1	Input buffer (I/O Address 60H) full. 0 = No data from the CPU in the input buffer. 1 = Data from the CPU in the input buffer. This bit is set to 0 when the keyboard controller reads the buffer.
2	System flag 0 = Power-on reset occurred. 1 = Self-test successful
3	Command/data 0 = A data byte written (port 60H) 1 = A command byte written (port 64H)
4	Front panel keylock status 0 = Keyboard inhibited 1 = Keyboard not inhibited
5	Auxiliary (mouse) device output buffer full. 0 = Output buffer is keyboard device data. 1 = Output buffer is auxiliary device data.
6	General time-out. 0 = Data reception from the keyboard/auxiliary device terminated normally within the programmed time-out delay. 1 = Data from the keyboard/auxiliary device did not terminate normally within the programmed time-out delay.

Table 12-1. Status Register Bit Definition *(continued)*

Bit	Function
7	Parity error. 0 = Last byte of data received from the keyboard/auxiliary device had odd parity (no error). 1 = Last byte of data received from the keyboad/auxiliary device had even parity (error).

12.2.2 Output Buffer

The controller output buffer is an 8-bit read-only register at I/O address 60H. The controller sends keyboard scan codes, command requested data bytes, and mouse data to the system via the output buffer. The significant data in the output buffer can be read only when the output buffer full bit (bit 0) of the status register equals 1.

12.2.3 Input Buffer

The controller input buffer is an 8-bit write-only register at I/O addresses 60H and 64H. Data can be written to the input buffer only if the input buffer full bit (bit 1) of the status register equals 0.

Writing to address 60H clears the command/data bit (bit 3) of the status register. Once cleared, the controller processes the data in the input buffer as a data byte. Data written to address 60H is sent to the keyboard, unless a system command instructs the controller to wait for a data byte.

Writing to address 64H sets the command/data bit (bit 3) of the status register to 1. Once set, the controller processes the data in the input buffer as a command byte.

12.2.4 Input and Output Ports

The input port consists of two signals to the controller driven by the keyboard and mouse and two signals indicating the keylock state and color/monochrome bit setting. The output port consists of eight signals driven by the controller to the keyboard, mouse, or system interface. These ports are accessed by sending the appropriate read or write command to the controller. Tables 12-2 and 12-3 list the input and output port bit assignments respectively.

Table 12-2. Input Port Bit Assignments

Bit	Function
7	Keylock (lock = 0)
6	Color/mono (color = 0)
5	MFG TEST (enabled = 0)
4:2	Reserved
1	Mouse data in
0	Keyboard data in

Table 12-3. Output Port Bit Assignments

Bit	Function
7	Keylock (lock = 0)
6	Color/mono (color = 0)
5	MFG TEST (enabled = 0)
4:2	Reserved
1	Mouse data in
0	Keyboard data in

12.3 CONTROLLER COMMANDS

The CPU uses controller commands (refer to Table 12-4) to control the operation of the controller and sense its status. The CPU writes controller commands into the input buffer through I/O port address 64H.

Table 12-4. Controller Commands

Code	Description
20H	Read controller command byte
21H:3FH	Read 8742 internal RAM locations 21-3FH
60H	Write controller command byte
61H:7FH	Write internal RAM locations 21-3FH
A7H	Disable auxiliary device (mouse)
A8H	Enable auxiliary device
A9H	Auxiliary interface test
AAH	Self-test
ABH	Keyboard test interface
ADH	Disable keyboard
AEH	Enable keyboard
C0H	Read input port
C1H	Poll input port low
C2H	Poll input port high
D0H	Read output port
D1H	Write output port
D2H	Write keyboard output buffer
D3H	Write auxiliary output buffer
D4H	Write to auxiliary device
E0H	Read test input port
E1H:EFH	Set/clear output pin
F0H:FFH	Output pulse

12.4 KEYBOARD/MOUSE INTERFACE

The keyboard and mouse connect to the controller through bidirectional synchronous serial interface cables. Refer to Appendix E for the pin assignments of the keyboard and mouse connectors. The controller supplies the keyboard and mouse with DC power of +5V±10% at a maximum current of 300mA.

The controller, keyboard, and mouse communicate using data and clock lines for synchronous serial communication. Open-collector drivers, at both ends of the cable, drive the data and clock lines.

At power-up, the keyboard scans the signals on the clock and data lines and establishes a line protocol. A bidirectional serial interface in the keyboard converts the clock and data signals and transfers them to and from the keyboard through the keyboard cable. Signals include keyboard control commands from the system and keyboard scan and acknowledgement codes transferred to the controller.

The serial data from the keyboard is called a scan code. Each keyboard key has an associated 11-bit scan code. Pressing and releasing a key generates a make or break scan code. The keyboard detects all keys pressed and transfers each scan code in the correct sequence to the controller.

The controller receives serial data form the keyboard, checks the parity of the data, and translates the 8-bit scan code into system codes. It also interrupts the CPU to transfer data to the system. The controller interrupts the system when data is placed in its output buffer, or waits for the system to poll its status register to determine when data is available.

The controller transfers various commands to the keyboard at any time. When the controller transfers data to the keyboard, it sets the data line to an inactive state and allows the clock line to go active. This action serves as a request-to-send (RTS) and a start bit. Setting the clock line to an inactive state inhibits keyboard transmission.

If the controller has to transfer data to the keyboard during a keyboard transfer, the controller clamps the clock signal line to request a keyboard transfer half. The clock line must remain low for at least 60 ms.

During the keyboard basic assurance test (BAT) or when no data transfer occurs, the clock line remains active (high). The keyboard holds the data line active (high).

An inactive signal has a value between 0V and +0.7V (logical 0). An active signal has a value between +2.4V and +5.5V (logical 1). These voltages are measured between a signal source and the DC network ground.

12.4.1 Keyboard/Mouse Data Stream

The 8-bit data steam, transferred serially over the data line, consists of one start bit, eight data bits, one odd parity bit, and one stop bit (refer to Table 12-5). A logic 1 indicates an active level and a logic 0 indicates an inactive level. The parity bit is either 1 or 0. The 8 data bits plus the parity bit always have an odd number of 1's.

Table 12-5. Data Stream Bits

Bit	Function
1	Start bit (always 0)
2	Data bit 0 (LSB)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (MSB)
10	Parity bit (odd parity)
11	Stop bit (always 1)

12.4.2 Receiving Data from the Keyboard

The keyboard transfers data to the controller in a serial format using an 11-bit frame. The first bit is a start bit, followed by 8 data bits, an odd parity bit, and a stop bit. A clock, supplied by the keyboard, synchronizes the data transfer.

Before transferring data, the keyboard checks for a transmission-inhibit or controller RTS status on the clock and data lines. If transmission is inhibited (clock line inactive), keycodes are transferred to the keyboard buffer. During controller RTS, data is also stored in the keyboard buffer, while the keyboard receives controller data.

The keyboard transfers data to the controller only when both the clock and data signals are active. At the end of a transfer, the controller disables the interface until the system accepts the data byte.

If a parity check error occurs, the controller signals the keyboard to transfer the data again. If the controller does receive the data correctly (after a set number of retires), an FFH code is sent to the controller output buffer. The parity bit in the status register is also set indicating a receive parity error.

The controller times each data byte transfer from the keyboard. If a keyboard transfer does not end within 2 ms, the controller sets the receive time-out bit in the status register and writes an FFH code to its output buffer. No retries are attempted on a receive time-out error.

The following commands are sent from the keyboard to the controller.

OVERRUN OR KEY DETECTION ERROR (00H OR FFH)

If the keyboard uses scan code set 1, the code equals FFH. For sets 2 and 3, the code equals 00H. The conditions are as follows:

- The keyboard sends a key detection error character if conditions in the keyboard make it impossible to identify a switwch closure.
- When the buffer in the keyboard is full, an overrun character replaces the last transmitted code in the buffer. This code is sent to the controller when it reaches the top of the buffer queue.

KEYBOARD ID (83ABH)

The Keyboard ID consists of two bytes, 83ABH. The keyboard responds to the read ID with ACK, discontinues scanning, and sends the two ID bytes. The keyboard sends the low byte first, followed by the high byte. The keyboard resumes scanning following an output of the keyboard ID.

BAT COMPLETION CODE (AAH)

Each time the system is powered up, the keyboard performs a self-test operation called the basic assurance test (BAT). The BAT consists of a keyboard processor test, a checksum of the ROM, and a RAM test. Activity on the clock and data lines is ignored during BAT. The keyboard sends an AAH command to the controller following satisfactory completion of the BAT. Any other code indicates a keyboard failure.

BAT FAILURE CODE (FCH)

If a BAT follure occurs, the keyboard sends FCH, discontinues scanning, and waits for a controller response or reset.

ECHO (EEH)

When the controller issues the echo command to the keyboard, the keyboard sends EEH as a response to the controller.

ACKNOWLEDGE (EAH)

The keyboard issues an acknowledge to any valid input other than an echo or a resend command. If the keyboard is interrupted while sending an acknowledge, it discards acknowleldge and responds to the new command.

RESEND (FEH)

The keyboard sends the resend command when it receives an invalid input or any input with incorrect parity. This command signals the controller to transfer the input again.

12.4.3 Sending Data to the Keyboard

The controller transfers data to the keyboard in the same serial format used to receive data from the keyboard. Before the controller transfers data to the keyboard, it checks the keyboard and determines whether it is transferring data on not. If the keyboard is transferring data, but has not reached the tenth clock signal, the controller overrides the keyboard output by setting the keyboard clock line inactive. If the keyboard transfer is beyond the tenth clock signal, the controller waits until the keyboard completes its transfer before transferring data.

If the controller overrides the keyboard output, or if the keyboard is not transferring data, the controller sets the clock line inactive for more than 60 μs while preparing to transfer data. When the controller transfers the start bit, the clock line goes active.

Each controller command or data transmission to the keyboard requires a response before the controller its next output. After the keyboard receives a controller command, it returns an acknowledge code to the controller. If the keyboard response is invalid or has a parity error, FEH is placed in the controller output buffer and the transmit time-out or parity error bits are set in the status register.

The controller sets a programmed time limit (20 ms to 25 ms) for the keyboard to respond. If the keyboard cannot complete the send-out data process within this time period, the controller places FEH in its output buffer and sets the transmit and receive time-out error bits in its status register. No retries are attempted by the controller for any transmission error. The following commands are sent from the controller to the keyboard.

SET/RESET STATUS INDICATORS (EDH)

The set/reset status indicators command activates or deactivates the three LED indicators (Num Lock, Caps Lock, and Scroll Lock) on the keyboard.

The keyboard responds to the command byte with ACK, discontinues scanning, and waits for the option byte from the controller. The contents of the option byte following the command determines the parameter for setting the LED mode. Bits 0, 1, and 2 of this byte control the Scroll Lock, Num Lock, and Caps Lock LEDs respectively. Bits 3 through 7 are reserved.

If the bit for an indicator equals 1, the indicator turns on. If the equals 0, the indicator turns off. The keyboard responds to the option byte with an acknowledge code, sets the indicators, and resumes scanning.

ECHO (EEH)

The echo command tests the keyboard command process. When the keyboard receives this command, it issues an EEH response, and continues scanning.

INVALID COMMAND (EFH AND F1H)

EFH and F1H are invalid commands.

SELECT ALTERNATE SCAN CODES (F0H)

The select alternate scan codes command instructs the keyboard to select one of three sets of scan codes. The keyboard acknowledges receipt of this command with an acknowledge code, then clears both the output buffer and the typematic key (if active). When the controller sends the option byte, the keyboard responds with another acknowledge code. An option byte value of 01H selects scan code set 1, 02H selects set 2, and 03H selects set 3. Byte value 00H causes the keyboard to respond with an acknowledge code and send a byte signaling the controller which scan code set is in use.

READ ID (F2H)

The read ID command requests identification information from the keyboard. The keyboard responds with an acknowledge code, discontinues scanning, and ends the two keyboard ID bytes. The second byte must follow completion of the first byte within 500 μs. After the output of the second ID byte, the keyboard resumes scanning.

SET TYPEMATIC RATE/DELAY (F3H)

This command sets the typematic rate and delay. The keyboard responds with an acknowledge code, stops scanning, and waits for the controller to issue the rate/delay value byte. Once issued, the keyboard responds with another acknowledge code, sets the rate and delay to the values indicated, and resumes scanning.

The contents of the rate/delay value byte following the command determines the parameters for these two functions. Bits 4:0 set the typematic rate, bits 5 and 6 set the delay parameter, and bit 7 is set to zero.

The following equations show the calculation for the delay and the typematic rate:

- Delay = $(1+C)\times 250$ ms$\pm$20%
- Period T = $(8+A)\pm 2^B \times 0.00417$ seconds
- Typematic Rate = $1/T\pm$20% (default is 10 characters per second)

Where: C = Binary value of bits 5 and 6 (default equals 500 ms)
A = Binary value of bits 2, 1, and 0
B = Binary value of bits 4 and 3
T = Interval from one typematic output to the next

ENABLE (F4H)

When the keyboard receives the enable command, it responds with an acknowledge code, clears its output buffer, clears the last typematic key, and starts scanning.

DEFAULT DISABLE (F5H)

The default disable command resets all conditions to the power-on default state. The keyboard responds with an acknowledge code, clears its output buffer, sets the default key types and typematic rate/delay, and clears the last typematic key. The keyboard stops scanning and waits for further instructions from the controller.

SET DEFAULT (F6H)

The set default command is similar to default disable command F5H. However, the keyboard continues scanning instead of stopping and waiting for further instructions.

SET ALL KEYS (F7H, F8H, F9H, FAH)

The sets all keys commands, F7H, F8H, F9H, and FAH, instruct the keyboard to set all keys to typematic, make/break, make, and typematic/make/break respectively. The keyboard responds with an acknowledge code, clears its output buffer, sets all keys to the type indicates by the command, and continues scanning. Although these commands are sent using any scan code set, they affect only scan code set 3.

SET KEY TYPE (FBH, FCH, FDH)

The set key type commands, FBH, FCH, and FDH, instruct the Keyboard to set individual keys to typematic, make/break, and make respectively. The keyboard responds with an acknowledge, clears its output buffer, and prepares to receive key identification. The controller identifies each key by its scan code value as defined in scan code set 3. Only scan code set 3 values are valid for key identification. The type of each identified key is set to the value indicated by the command.

RESEND (FEH)

The controller transfers the resend command when it detects an error in any transfer from the keyboard. It requests the keyboard to resend a code that was detected as an error. This command transfers only after a keyboard transfer and before the controller allows the next keyboard output. When a resend command is received, the keyboard transfers the previous output again. If the previous output was resend, the keyboard transfers the last byte before the resend command.

RESET (FFH)

The controller issues the reset command to start a program reset and a keyboard internal self-test. The keyboard responds with an acknowledge code and ensures the controller accepts the acknowledge code before executing the command. The controller raises the clock and data lines for a minimum of 500 μs after receiving an acknowledge code from the keyboard. The keyboard remains disabled from the time it receives the reset command until the controller responds to the acknowledge code, or until another command overrides the previous command. After the controller responds to the acknowledge code, the keyboard initializes and performs the BAT. After returning the completion code the keyboard defaults to scan code set 2.

12.4.4 System-To-Mouse Commands

The write to auxiliary device command (D4H) instructs the 8742 to transmit the next byte it receives to the auxiliary device. All commands written to the mouse must be written must be preceded by the write to auxiliary device command to port 64H, followed by the desired mouse command. All mouse commands must be written to port 60H. If the write to auxiliary device command to port 64H is not executed first, all mouse commands will be directed to the keyboard.

RESET SCALING (E6H)

The reset scaling command resets the scaling to 1:1.

SET SCALING (E7H)

The set scaling command sets the scaling to 2:1. This command can only be used when the mouse is in stream mode. When in stream mode, the current X/Y coordinates values are converted to new values each time the sample period expires. In 2:1 scaling, the new relationship between the input and output values is as follows:

Input	Output
0	0
1	1
2	1
3	3
4	6
5	9
N (>=6)	2.0×N

SET RESOLUTION (E8H)

The set resolution command is a two byte command. The second byte (also written to port 60H) is interpreted as a resolution in counts per mm. There are four possible resolutions. The relationship between the second byte and the resolution is as follows:

Byte	Resolution
00H	1 count per mm
01H	2 counts per mm
02H	4 counts per mm
03H	8 counts per mm

STATUS REQUEST (E9H)

The status request command generates a three byte status report. The format of the mouse status request bytes is shown in Table 12-6.

Table 12-6. Format of Status Request Bytes

Byte	Function
3	Sampling Rate Bit 7 = Most significant bit Bit 0 = Least signficiant bit
2	Resolution Bit 7 = Most significant bit Bit 0 = Least significant bit
1	Mouse status Bit 7 = Reserved Bit 6 = 0 Stream mode 1 Remote mode Bit 5 = 0 Disabled 1 Enabled Bit 4 = 0 Scaling 1:1 1 Scaling 2:1 Bit 3 = Reserved Bit 2 = 1 Left mouse button pressed Bit 1 = Reserved Bit 0 = 1 Right mouse button pressed

SET STREAM MODE (EAH)

In set stream mode, the mouse transmits data to the system each time a mouse button is pressed or released, or each time the mouse detects a unit of movement. the mouse data sample rate determines the maximum number of times per second that mouse data can be transmitted to the system. If no button is pressed or if the mouse is not moved, no data is transmitted. The set stream mode command enables the stream mode.

READ DATA (EBH)

The read data command forces the transmission of one mouse data packet. The read data command is valid in both stream mode and remote mode.

RESET WRAP MODE (ECH)

The reset wrap mode command resets the mouse to normal operation.

SET WRAP MODE (EEH)

This command sets wrap mode; the mouse echo mode. With the exception of the reset wrap mode (ECH) and reset mouse (FFH) commands, the mouse will echo all data and commands received from the system.

SET REMOTE MODE (F0H)

This command sets remote mode; the mouse data can only be transmitted in reply to a read data command.

READ DEVICE TYPE (F2H)

The read device type command reads the mouse ID byte. The mouse returns a value of 00H to the read device command.

SET SAMPLING RATE (F3H)

This command sets the sampling rate of the mouse. The sampling rate is defined as the number of times per second that the system checks for mouse data. This is a two byte command. The set sampling rate command (F3H) must be followed by a second byte that represents the hex value of the sampling rate. The allowable values are defined below:

Hex Value	Sampling Rate
0AH	10 samples/second
14H	20 samples/second
28H	40 samples/second
3CH	60 samples/second
50H	80 samples/second
64H	100 samples/second
C8H	200 samples/second

ENABLE (F4H)

The enable command enables data transmissions if the mouse has been set to stream mode. This command has no effect in remote mode.

DISABLE (F5H)

The disable command disables data transmissions if the mouse has been set to stream mode. This command has no effect in remote mode.

SET DEFAULT (F6H)

The set default command reinitializes the mouse to its power-on default state. The mouse power-on default state is shown below:

Sampling rate	100 samples/second
Scaling	Linear scaling
Mode	Stream mode
Resolution	4 counts/mm
Transmissions	Disabled

RESEND (FEH)

The resend command is issued by the system in response to transmission errors from the mouse. The mouse responds to this command by retransmitting its last data packet.

RESET (FFH)

The reset command instructs the mouse to run its internal self-test routine. This command puts the mouse into reset mode.

12.4.5 Mouse-To-System Replies

There are two mouse-to-system replies. Both replies are related to command processing and are read by the system at port 60H.

ACKNOWLEDGE (FAH)

The mouse replies with an acknowledge (FAH) whenever it receives a valid command from the system. Unlike mouse serial data packets, the acknowledge reply is not stored in a buffer in internal memory, but is discarded immediately after it is transmitted. If a new command is received while the mouse is in the acknowledge reply process, the mouse discards the acknowledge reply and begins processing the new command immediately.

Note: The reset wrap mode (ECH) and reset (FFH) commands are exceptions to mouse acknowledge response. The mouse does not respond with an acknowledge to either of these commands.

RESEND (FEH)

The mouse replies with a resend (FEH) when it receives an invalid command from the system. Two invalid commands in succession cause the mouse to send the error code FCH to the system. A single isolated invalid command does not affect mouse processing in any way. The mouse ignores single invalid commands and maintains its present operational state.

SET WRAP MODE (EEH)

This command sets wrap mode; the mouse echo mode. With the exception of the reset wrap mode (ECH) and reset mouse (FFH) commands, the mouse will echo all data and commands received from the system.

SET REMOTE MODE (F0H)

This command sets remote mode; the mouse data can only be transmitted in reply to a read data command.

READ DEVICE TYPE (F2H)

The read device type command reads the mouse ID byte. The mouse returns a value of 00H to the read device command.

SET SAMPLING RATE (F3H)

This command sets the sampling rate of the mouse. The sampling rate is defined as the number of times per second that the system checks for mouse data. This is a two byte command. The set sampling rate command (F3H) must be followed by a second byte that represents the hex value of the sampling rate. The allowable values are defined below:

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64H	100 samples/second
C8H	200 samples/second

ENABLE (F4H)

The enable command enables data transmissions if the mouse has been set to stream mode. This command has no effect in remote mode.

DISABLE (F5H)

The disable command disables data transmissions if the mouse has been set to stream mode. This command has no effect in remote mode.

SET DEFAULT (F6H)

The set default command reinitializes the mouse to its power-on default state. The mouse power-on default state is shown below:

Sampling rate	100 samples/second
Scaling	Linear scaling
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Resolution	4 counts/mm
Transmissions	Disabled

RESEND (FEH)

The resend command is issued by the system in response to transmission errors from the mouse. The mouse responds to this command by retransmitting its last data packet.

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The reset command instructs the mouse to run its internal self-test routine. This command puts the mouse into reset mode.

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13

DP8473 FLOPPY DISK CONTROLLER

13.1 INTRODUCTION

This device is a derivative of the DP8472/4 Floppy Disk Controller which incorporates additional logic specifically required for an IBM® PC, PC-XT®, PC-AT®, or PS/2® design. This controller is a full featured floppy disk controller that is software compatible with the μPD765A, but also includes many additional hardware and software enhancements.

This controller incorporates a precision analog data separator, that includes a self trimming delay line and VCO. Up to three external filters are switched automatically depending on the data rate selected. This provides optimal performance at the standard PC data rates of 250/300 kb/s, and 500 kb/s. It also enables optimum performance at 1 Mb/s (MFM). These features combine to provide the lowest possible PLL bandwidth, with the greatest lock range, and hence the widest window margin.

The controller includes write precompensation circuitry. A shift register is used to provide a fixed 125ns early-late precompensation for all tracks at 500k/300k/250 kb/s (83ns for 1 MB/s), or a precompensation value that scales with the data rate, 83ns/125ns/208ns/250ns for data rates of 1.0M/500k/300k/250 kb/s respectively.

Specifically to support the PC-AT and PC-XT design, the Floppy Disk Controller PLUS-2 includes address decode for the A0-A2 address lines, the motor/drive select register, data rate register for selecting 250/300/500 kb/s, Disk Changed status, dual speed spindle motor control, low write current and DMA/interrupt sharing logic. The controller also supports direct connection to the μP bus via internal 12 mA buffers. The controller also can be connected directly to the disk drive via internal open drain high drive outputs, and Schmitt inputs.

In addition to this logic the DP8473 includes many features to ease design of higher performance drives and future controller upgrades. These include 1.0 Mb/s data rate, extended track range to 4096, Implied seeking, working Scan Commands, motor control timing, both standard IBM formats as well as Sony 3.5" (ISO) formats, and other enhancements.

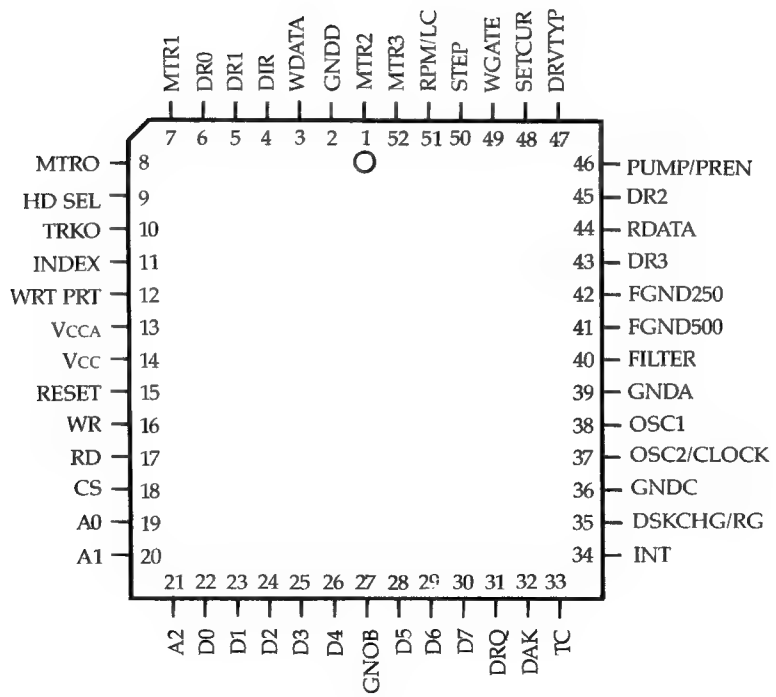
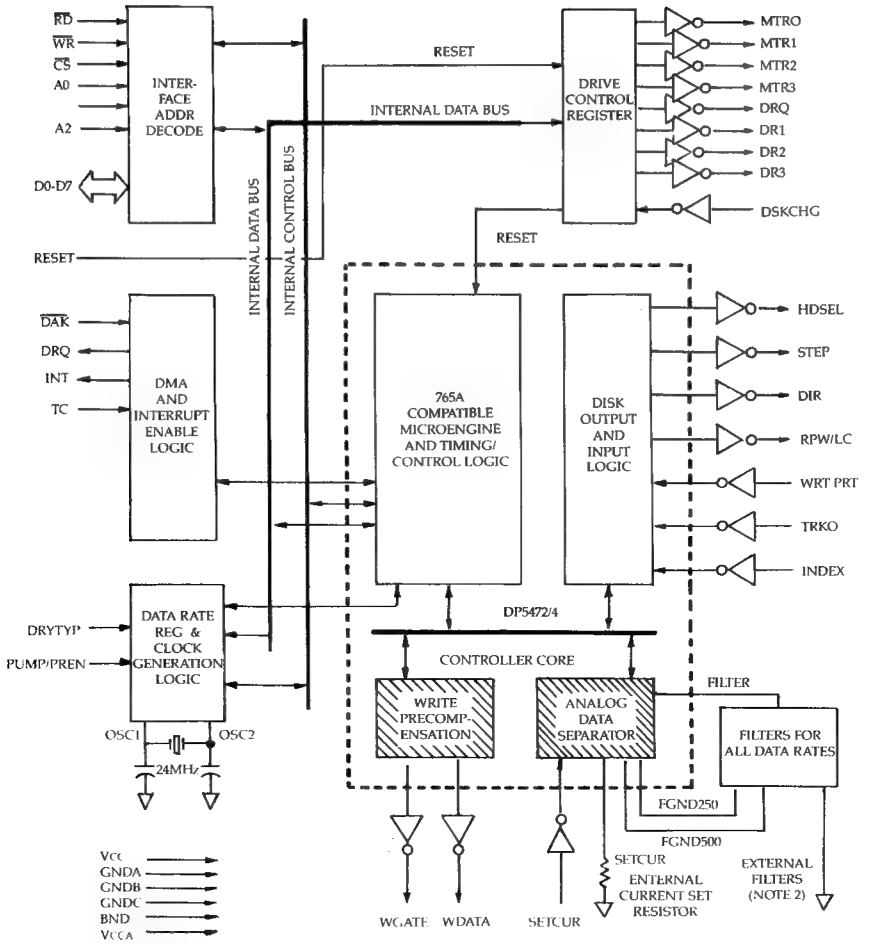


Figure 13-1. Connection Diagrams

13.2 FEATURES

- Fully μPD765A and IBM-BIOS compatible
- Integrates all PCXT®, PCAT®, and most PS/2® Logic
  - — On chip 24MHz Crystal Oscillator
  - — DMA enable logic
  - — IBM compatible address decode of A0-A2
  - — 12 mA μP bus interface buffers
  - — 40 mA floppy drive interface buffers
  - — Data rate and drive control registers
- Precision analog data separator
  - — Self-calibrating PLL and delay line
  - — Automatically chooses one of three filters
  - — Intelligent read algorithm
- Two pin programmable precompensation modes
- DP8472/4 core with its enhancements
  - — Up to 1 Mb/s data rate
  - — Implied seek up to 4000 tracks
  - — IBM or ISO formatting
- Low power CMOS, with power down mode



Note 1: The MTR2, MTR3, DR2, and DR3 are not available on the 48 pin DIP (DP8473N, J) versions.

Note 2: See *Figure 4* for filter description.

Note 3: Total transistor count is 29,700 (approx).

Figure 13-2. DP8473 Functional Block Diagram

13.3 PIN DESCRIPTIONS

Symbol	Function
MTR2	This is an ctive low motor enable line for drive 2, which is controlled by the Drive Control register. This is a high drive open drain output.
GNDD	This pin is the digital ground for the disk interface output drivers.
WDATA	This is the active low open drain write precompensated serial data to be written onto the selected disk drive. This is a high drive open drain output.
DIR	This output determines the direction of the head movement (low = step in, high = step out). When in the write or read modes, this output will be high. This is a high drive open drain output.
DR1	This is an active low drive select line for drive 1 that is controlled by the Drive Control register bits D0, D1. The Drive Select bit is ANDed with the Motor Enable of the same number. This is a high drive open drain output.
DR0	This is an active low drive select similar to DR1 line except for drive 0.
MTR1	This is an active low motor enable line for drive 1. Similar to MTR2.
MTR0	This is an active low motor enable line for drive 0. Similar to MTR2.
HD SEL	This output determines which disk drive head is active. Low = Head 1, Open (high) = Head 0. This is a high drive open drain output.
TRK0	This active low Schmitt input tells the controller that the head is at track zero of the selected disk drive.
INDEX	This active low Schmitt input signals the beginning of a track.
WRT PRT	This active low Schmitt input indicates that the disk is write protected. Any command that writes to that disk drive is inhibited when a disk is write protected.
VCCA	This pin is the 5V supply for the analog data separator circuitry.
VCC	This pin is the 5V supply for the digital circuitry.
RESET	Active high input that resets the controller to the idle state, and resets all the output lines to the disk drive to their disabled state. The Drive Control register is reset to 00. The Data Rate register is set to 250 kb/s. The Specify command registers are not affected. The Mode Command registers are set to the default values. Reset should be held active during power up. To prevent glitches activating the reset sequence, a small capacitor (1000 pF) should be attached to this pin.

Symbol	Function
WR	Active low input to signal a write from the microprocessor to the controller.
RD	Active low input to signal a read from the controller to the microprocessor.
CS	Active low input to enable the RD and WR inputs. Not required during DMA transfers. This should be held high during DMA transfers.
A0, A1, A2	Address lines from the microprocessor. This determines which registers the microprocessor is accessing as shown in Table IV in the Register Description Section. Don't care during DMA transfers.
D0-D4	Bi-directional data lines to the microprocessor. These are the lower 5 bits and have buffered 12 mA outputs.
GNDB	This pin is the digital ground for the 12 mA microprocessor interface buffers. This includes D0-D7, INT, and DRQ.
D5-D7	Bi-directional data lines to the microprocessor. These upper 3 bits have buffered 12 mA outptus.
DRQ	Active high output to signal the DMA controller that a data transfer is needed. This signal is enabled when D3 of the Drive Control Register is set.
DAK	Active low input to acknowledge the DMA request and enable the RD and WR inputs. This signal is enabled when D3 of the Drive Control Register is set.
TC	Active high input to indicate the termination of a DMA transfer. This signal is enabled when the DMA Acknowledge pin is active.
INT	Active high output to signal that an operation requires the attention of the microprocessor. The action required depends on the current function of the controller. This signal is enabled when D3 of the Drive Control Register is set.
DSKCHG/RG	This latched Schmitt input signal is inverted and routed to D7 of the data bus and is read when address xx7H is enabled. When the RG bit in the Mode Command is set, this pin functions as a Read Gate signal that when low forces the data separator to lock to the crystal, and when high it locks to data for diagnostic purposes.
GNDC	This pin is the digital ground for the controller's digital logic, including all internal registers micro-engine, etc.

Symbol	Function
OSC2/CLOCK	One side of the external 24MHz crystal is attached here. If a crystal is not used, a TTL or CMOS compatible clock is connected to this pin.
OSC1	One side of an external 24MHz crystal is attached here. This pin is tied low if an external clock is used.
GNDA	This pin is the analog ground for the data separator, including all the PLLs, and delay lines.
FILTER	This pin is the output of the charge pump and the input to the VCO. One or more filters are attached between this pin and the GNDA, FGND250 and FNGD500 pins.
FGND500	This pin connects the PLL filter for 500k(MFM)/250k(FM) b/s to ground. This is a low impedance open drain output.
FGND250	This pin connects the PLL filter for 250k(MFM)/125k(FM) b/s or 300k(MFM)/ 150k(FM) b/s to ground. This is a low impedance open drain output.
DR3	This is the same as DR0 except for drive 3.
RDATA	The active low raw data read from the disk is connected here. This is a Schmitt input.
DR2	This is the same as DR0 except for drive 2.
PUMP/PREN	When the PU bit is set in Mode Command this pin is an output that indicates when the charge pump is making a correction. Otherwise this pin is an input that sets the precomp mode as shown in Table VI. If pin is configured as PUMP, PREN is assumed high.
DRV TYP	This is an input used by the controller to enable the 300 kb/s mode. This enables the use of floppy drives with either dual or single speed spindle motors. For dual speed spindle motors, this pin is tied low. When low, and 300 kb/s data rate is selected in the data rate register, the PLL actually uses 250 kb/s. This pin is tied high for single speed spindle motor drives (standard AT drive). When this pin is high and 300 kb/s is selected 300 kb/s is used. (See also RPM/LC pin).
SETCUR	An external resistor connected from this pin to analog ground programs the amount of charge pump current that drives the external filters. The PLL Filter Design section shows how to determine the values.

Symbol	Function
WGATE	This active low open drain high drive output enables the write circuitry of the selected disk drive. This output has been designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled.
STEP	This active low open drain high drive output will produce a pulse at a software programmable rate to move the head during a seek operation.
RPM/LC	This high drive open drain output pin has two functions based on the selection of the DRVTYP pin. 1. When using a dual speed spindle motor floppy drive (DRVTYP pin low), this output is used to select the spindle motor speed, either 300 RPM or 360 RPM. In this mode this output goes low when 250/300 kb/data rate is chosen in the data rate register, and high when 500 kb/s is chosen. 2. When using a single speed spindle motor floppy drive (DRVTYP pin high), this pin indicates when to reduce the write current to the drive. This output is high for high density media (when 500 kb/s is chosen).
MTR3	This is an active low motor enable line for drive 3.

Typical Application

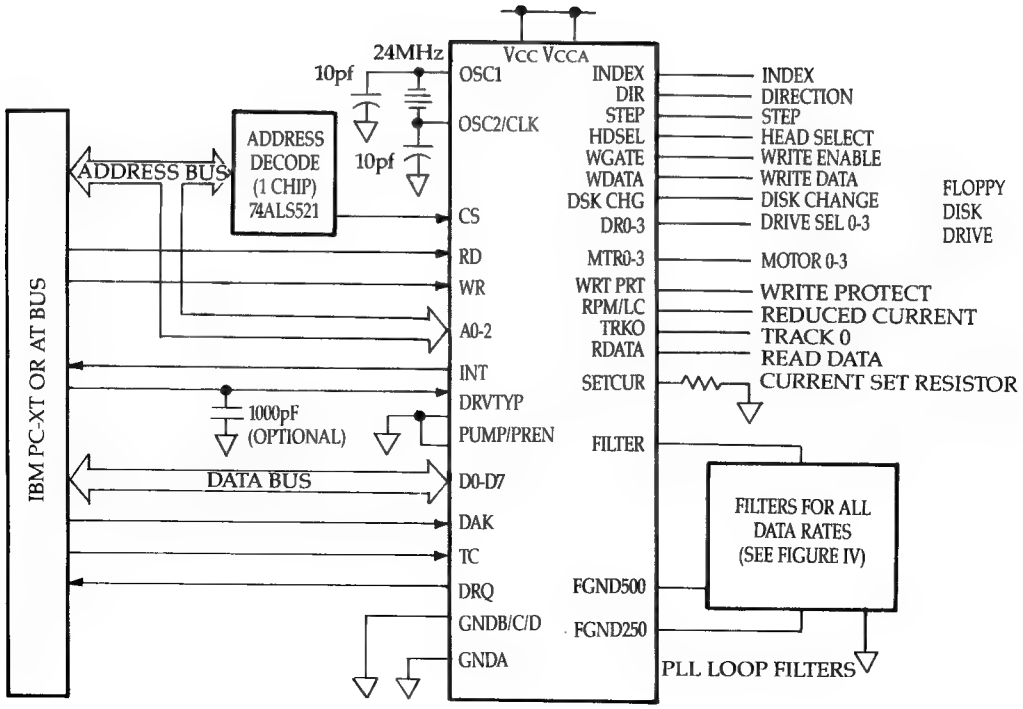


Figure 13-3. DP8473 Typical Application

13.4 FUNCTIONAL DESCRIPTIONS

This section describes the basic architectural features of the DP8473, and many of the enhancements provided. Refer to *Figure 13-2*.

13.4.1 765A Compatible Micro-Engine

The core of the DP8473 is the same μPD765A compatible microcoded engine that is used in the DP8472/4. This engine consists of a sequencer, program ROM, and disk/misc registers. This core is clocked by either a 4MHz, 4.8MHz or 8MHz clock selected in the Data Rate Register. Upon this core is added all the glue logic used to implement a PC-XT or AT, or PS/2 floppy controller, as well as the data separator and write precompensation logic.

The controller consists of a microcoded engine that controls the entire operation of the chip including coordination of data transfer with the CPU, controlling the drive controls, and actually performing the algorithms associated with reading and writing data to/from the disk. This includes the read algorithm for the data separator.

Like the μPD765A, this controller takes commands and returns data and status through the Data Register in a byte serial fashion. Handshake for command/status I/O is provided via the Main Status Register. All of the μPD765A commands are supported, as are many of the DP8472 superset commands.

13.4.2 Data Separator

The internal data separator consists of an analog PLL and its associated circuitry. The PLL synchronizes the raw data signal read from the disk drive. The synchronized signal is used to separate the encoded clock and data pulses. The data pulses are de-serialized into bytes and then sent to the μP by the controller.

The main PLL consists of four main components, a phase comparator, a filter, a voltage controlled oscillator (VCO), and a programmable divider. The phase comparator detects the difference between the phase of the divider's output and the phase of the raw data being read from the disk. This phase difference is converted to a current which either charges or discharges one of the three external filters. The resulting voltage on the filter changes the frequency of the VCO and the divider output to reduce the phase difference between the input data and the divider's output. The PLL is "locked" when the frequency of the divider is exactly the same as the average frequency of the data read from the disk. A block diagram of the data separator is shown in *Figure 13-4*.

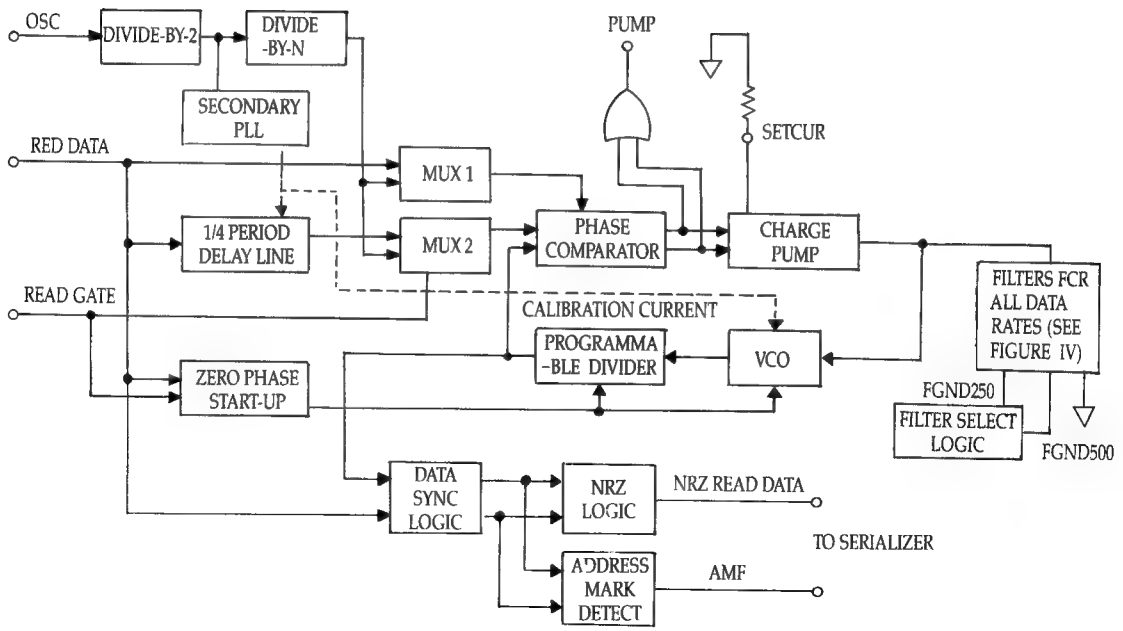
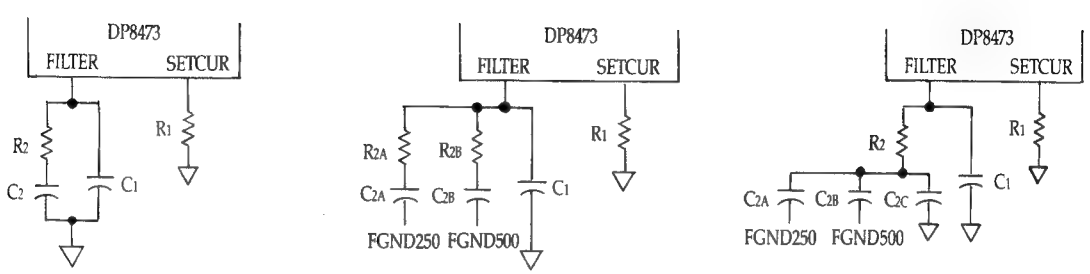


Figure 13-4. Block Diagram of DP8473's Data Separator



a) Single Data Rate **b) 250/500 kb/s Filter** **c) 250/500 kb/s and 1 Mb/s**

Note: For all filter configurations, 250 kb/s and 300 kb/s share the same filter.

Figure 13-5. Typical Configuration for Loop Filters for the DP8473 Showing Component Labels

To ensure optimal performance, the data separator incorporates several additional circuits. The quarter period delay line is used to determine the center of each bit cell. A secondary PLL is used to automatically calibrate the quarter period delay line. The secondary PLL also calibrates the center frequency of the VCO.

To eliminate the logic associated with controlling multiple data rates the DP8473 supports the connection of three filters to the chip via the FGND250, and FGND500 pins (filter ground switches). The controller chooses which filter components to use based on the value loaded in the Data Rate Register. If 500k(MFM) is being used then the FGND500 is enabled (FGND250 is disabled). If 250k(MFM) or 300k(MFM) is being used the FGND250 pin is enabled, and FGND500 is disabled. For 1 Mb/s (MFM) both FGND pins are disabled.

Figure 13-5 shows several possible filter configurations. For a filter to cover all data rates (*Figure 13-5*), the DP8473 has a 1 Mb/s filter always connected and other capacitor filter components for the other data rates are switched in parallel to this filter. The actual loop filter for 500 kb/s is the parallel combination of the two capacitors, C_{2C} and C_{2B}, attached to the FGND500 pin and to ground. The 250/300 kb/s filter is the parallel combination of the capacitors, C_{2C} and C_{2A}, attached to the FGND250, and ground. If 1 Mb/s need not be supported then the filter configuration of *Figure 13-5* can be used. This configuration allows more optimal performance for both 500k and 250/300 kb/s. *Figure 13-5* is a simple filter configuration primarily for a single data rate (or multiple data rates with a performance compromise). Table II shows some typical filter values. Other filter configurations and values are possible, these result in good general performance.

While the controller and data separator support both FM and MFM encoding, the filter switch circuitry only supports the IBM standard MFM data rates. The provide both FM and MFM filters external logic may be necessary.

The controller takes best advantage of the internal data separator by implementing a sophisticated ID search algorithm. This algorithm, shown in *Figure 13-6*, enhances the PLL's lock characteristics by forcing the PLL to relock to the crystal any time the data separator attempts to lock to a non-preamble pattern. This algorithm ensures that the PLL is not thrown way out of lock by write splices or bad data fields.

Table 13-1. Typical Filter Values for the Various Data Rates (Assuming ±6% Capture Range)

Data Rate (MFM b/s)	C_2	R_2	C_1	R_1
Filter Values when Using All 3 Data Rates				
1.0M 500k 250/300k	C_{2C} = 0.012μF C_{2B} = 0.015μF C_{2A} = 0.033μF	560Ω	510pF	5.6kΩ
Filter Values when Using 250/300 and 500 kb/s				
500k 250/300k	C_{2B} = 0.027μF C_{2A} = 0.047μF	560Ω 560Ω	1000pF	5.6kΩ
Filter Using Only One Data Rate				
1.0M	C_2 = 0.012μF	560Ω	510pF	5.6kΩ
500k	C_2 = 0.027μF	560Ω	1000pF	5.6kΩ
300/250k	C_2 = 0.047μF	560Ω	2000pF	5.6kΩ

(These values are preliminary and thus are subject to change.)

Table 13-2. Data Rates (MFM) Versus VCO Divide-By Factor

Data Rate	N
1 Mb/s	4
500 kb/s	8
300 kb/s	16
250 kb/s	16

13.4.3 PLL Diagnostic Modes

In addition, the DP8473 has two diagnostic modes to enable filter optimization, 1) enabling the Charge Pump output signal onto the PUMP/PREN pin, and 2) providing external control of the Read Gate signal to the data separator. Both modes are enabled in the last byte of the Mode Command.

The Pump output signal indicates when the charge pump is making a phase correction, and hence whether the loop is locked or not.

The Read Gate function, when enabled, allows the designer to manually force the data separator to lock to the incoming data or back to the reference clock. This enables easy verification of the lock characteristics of the PLL, by monitoring the FILTER pin, and the Pump signal.

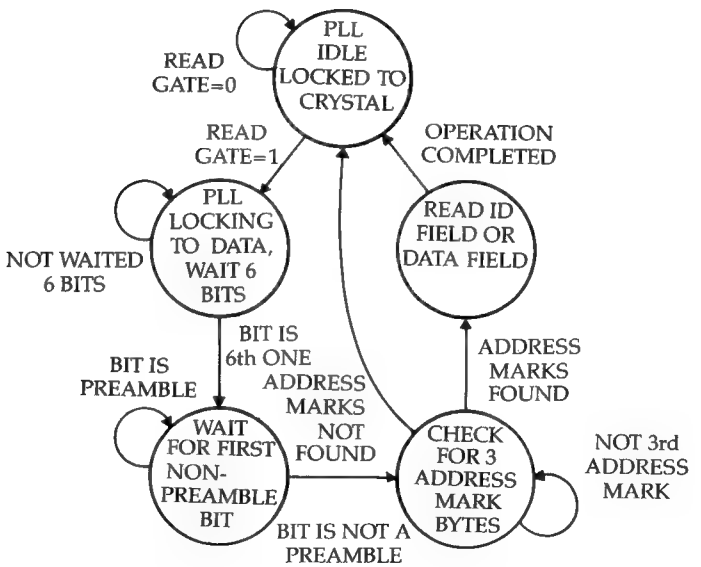


Figure 13-6. Read Algorithm-State Diagram for Data

13.4.4 PLL Filter Design

This section provides information to enable design of the data separator's external filter and charge pump set resistor. This discussion is for a single data rate filter, and can be easily extrapolated to the other filters of *Figure 13-5*. Table 13-1 shows some typical filter component values, but if a custom filter is desired, the following parameters must be considered:

R1 Charge pump current setting resistor. The current set by this resistor is multiplied by the charge pump gain, K_P which is ~2.5. Thus the charge pump current is:

$I_{PUMP} = (2.5)\ 1.2V/R1$. R1 should be set to between 3-12 kΩ. This resistor determines the gain of the phase detector, which is $K_D = I_{PUMP}/2\pi$.

C2 Filter capacitor in series with R2. With pump current this determines loop bandwidth.

R2 Filter resistor. Determines the PLL damping factor.

C1 This filter capacitor improves the performance of the PLL by providing additional filtering of bit jitter and noise.

K_{VCO} The ratio of the change in the frequency of the VCO output due to a voltage change at the VCO input. $K_{VCO} \approx 25$ Mrad/s/V. The VCO is followed by a divider to achieve the desired frequency for each data rate. VCO center frequency is 4MHz for data rates of 1 Mb/s, 500 kb/s, and 250 kb/s (MFM), and is 4.8MHz for 300 kb/s (MFM).

K_{PLL} This is the gain of the internal PLL circuitry, and is the product of $V_{REF} \times K_{VCO} \times K_P$. This value is specified in the Phase Locked Loop Characteristics table.

ωn This is the bandwidth of the PLL, and is given by,

$$\omega n = \frac{K_{PLL}}{2\pi C2N\ R1}$$

where N is the number of VCO cycles between two phase comparisons. The value of N for the various data rates are shown in Table 13-2.

ζ The damping factor is set to 0.7 to 1.2 and is given by,

$$\zeta = \frac{\omega n R2 C2}{2}$$

The trade off, when choosing filter components is between acquisition time while the PLL is locking and jitter immunity while reading data. To select the proper components for a standard floppy disk application the following procedure can be used:

1. Choose FM or MFM, and data rate. Determine N from Table 13-2. Determine preamble length (MFM = 12). The PLL should lock within 1/2 the preamble time.

2. Determine loop bandwidth (ωn) required, and set the charge pump resistor R1.

3. Calculate C2 using:

$$C2 = \frac{K_{PLL}}{2\pi R1 N \omega n2}$$

4. Choose R2 using:

$$R2 = \frac{2\zeta}{\omega n C2}$$

6. Select C1 to be about 1/20th of C2.

The above procedure will yield adequate loop performance. If optimum loop performance is required, or if the nature of the loop performance is very critical, then some additional consideration must be given to choosing ωn and the damping factor. (For a detailed description on how to choose ωn and ζ, see: **AN-505 Floppy Disk Data Separator Design Guide for the DP8472, DP8473, and DP8474).**

13.4.5 Write Precompensation

The DP8473 incorporates a single fixed 3-bit shift register. This shift register outputs are tapped and multiplexed onto the write data output. The taps are selected by a standard precompensation algorithm. This precompensation value can be selected from the PUMP/PREN pin. When this pin is low 125ns precomp is used for all data rates except 1 Mb/s which uses 83ns. When PREN is tied high, the precompensation-value scales with data rae at 250 kb/s its 250ns, at 300 kb/s its 208ns, at 500 kb/s its 125ns, and at 1.0 Mb/s its 83ns. These values are shown in Table 13-5.

13.4.6 PC-AT and PC-XT Logic Blocks

This section describes the major functional blocks of the PC logic that have been integrated on the controller. Refer to *Figure 13-2*, the block diagram.

DMA Enable Logic: This is gating logic that disables the DMA lines and the Interrupt output, under the control of the DMA Enable bit in the Drive control register. When the DMA Enable bit is 0 then the INT, and DRQ are held Tri-State and DAK is disabled.

Drive Output Buffers/Input Receivers: The drive interface output pins can drive 150Ω ±10% termination registors. This enables connection to a standard floppy drive. A drive interface inputs are TTL compatible schmitt trigger inputs with typically 250mV of hysteresis. *The only functional differences between the 52 pin PLCC and the 48 pin DIP version are that the MTR2 and 3, and DR2 and 3 pins have been removed in order to accommodate the 48 pin package.*

Bus Interface-Address Decode: The address decode circuit allows software access to the controller, Drive Control Register, and Data Rate Register (see Table 13-3 for the memory map) using the same address map as is used in the XT, AT, or PS/2. The decoding is provided for A0-A2, so only a single address decoder connected to the chip select is needed to complete the decode. The bus interface logic includes the 8-bit data bus and DRQ/INT signals. The output drive for these pins is 12mA.

Table 13-3. Address Memory Map for DP8473

A2	A1	A0	R/W	Register
0	0	0	X	None (Bus Tri-State)
0	0	1	X	None (Bus Tri-State)
0	1	0	W	Drive Control Register
0	1	1	X	None (Bus Tri-State)
1	0	0	R	Main Status Register
1	0	1	R/W	Data Register
1	1	0	X	None (Bus Tri-State)
1	1	1	W	Data Rate Register
1	1	1	R	Disk Changed Bit*

* When this location is accessed only bit D7 is driving, all others are head TRI-STATE.

Drive Control Register: This 8-bit write only register controls the drive selects, motor enables, DMA enable, and Reset. See Register Description.

Reset Logic: The reset input pin is active high, and directly feeds the Drive Control Register and the Data Rate Register. After a hardware reset the Drive Control Register is reset to all zeros, and the Data Rate Register is set to 250 kb/s data rate. The controller is held reset until the software sets the Drive Control reset bit, after which the controller may be initialized. A software reset to the controller core can be issued by resetting then setting this bit. A software reset does not reset the Drive Control Register, or the Data Rate Register.

Data Rate Register and Clock Logic: This is a two bit register that controls the data rate that the controller uses. See Register Description. This register feeds logic that selects the data rates by programming a prescaler that divides the crystal or clock input by either 3, 5, or 6. This causes either 4MHz, 4.8MHz and 8MHz to be input as the master clock for the controller core. If the Drive Type pin is high and a 300 kb/s data is chosen, 4.8MHz is used to generate 300 kb/s, but when the DRVTYP pin is low and 300 kb/s is selected, 4MHz is used, and the actual data rate is 250 kb/s. See Table 13-5.

Low Power Mode Logic: This logic is an enhancement over the standard XT, AT, PS/2 design. In the Low Power Mode the crystal oscillator, controller and all linear circuitry are turned off. When the oscillator is turned off the controller will typically draw about 100μA. The internal circuitry is disabled while the oscillator is off because the internal circuitry is driven from this clock. The oscillator will turn back on automatically after it detects a read or a write to the Main Status or Data Registers. It may take a few milli-seconds for the oscillator to stabilize and the μP will be prevented from trying to access the Data Register during this time through the normal Main Status Register will be inactive.) There are two ways to go into the low power mode. One is to command the controller to switch to low power immediately. The other method is to set the controller to automatically go into the low power mode 500ms after the beginning of the idle state (based on a 500 kb/s (MFM) data rate). This would be invisible to the software. The low power mode is programmed through the Mode Command.

The Data Rate Register and the Drive Control Register are unaffected by the power down mode. They will remain active. It is up to the user to ensure that the Motor and Drive select signal are turned off.

Table 13-4. Truth Table for Drive Control Register

D7	D6	D5	D4	D1	D0	Function
X	X	X	1	0	0	Drive 0 Selected (DR0 = 0)
X	X	1	X	0	1	Drive 1 Selected (DR1 = 0)
X	1	X	X	1	0	Drive 2 Selected (DR2 = 0)
1	X	X	X	1	1	Drive 3 Selected (DR3 = 0)

Crystal Oscillator: The DP8473 is clocked by a single 24MHz signal. An on-chip oscillator is provided, to enable the attachment of a crystal, or a clock. If a crystal is used, a 24MHz fundamental mode, parallel resonant crystal should be used. This crystal should be specified to have less than 150Ω series resistance, and shunt capacitance of less than 7pF. Typically a series resonant crystal can be used, it will just oscillate in parallel mode 30-300 ppm from its ideal frequency.

If an external oscillator circuit is used, it must have a duty cycle of at least 40-60%, and minimum input levels of 2.4V and 0.4V. The controller should be configured so that the clock is input into the OSC2 pin, and OSC1 is tied to ground.

Crystals: Staytek: CX1-SM1-24MHz(B)
SaRonix: SRX 3164

13.5 REGISTER DESCRIPTION

This section describes the register bits for all the registers that are directly accessible to the μP. Table 13-3 (previous page) shows the memory map for these registers. Note that in the PC some of the registers are partially decoded, this is not the case here. All registers occupy only their documented addresses.

13.5.1 Main Status Register (Read Only)

The read only Main Status Register indicates the current status of the disk controller. The Main Status Register is always available to be read. One of its functions is to control the flow of data to and from the Data Register. The Main Status Register indicates when the disk contoller is ready to send or receive data. It should be read before each byte is transferred to or from the Data Register except during a DMA transfer. No delay is required when reading this register after a data transfer.

D7 Request for Master: Indicates that the Data Register is ready to send or receive data from the μP. This bit is cleared immediately after a byte transfer and will become set again as soon as the disk controller is ready for the next byte.

D6 Data Direction: Indicates whether the controller is expecting a byte to be written to (0) or read from (1) the Data Register.

D5 Non-DMA Execution: Bit is set only during the Execution Phase of a command if, it is in the non-DMA mode. In other words, if this bit is set, the multiple byte data transfer (in the Execution Phase) must be monitored by the μP either through interrupts, or software polling as described in the Processor Software Interface section.

D4 Command In Progress: Bit is set after the first byte of the Command Phase is written. Bit is cleared after the last byte of the Result Phase is read. If there is no result phase in a command, the bit is cleared after the last byte of the Command Phase is written.

D3 Drive 3 Seeking: Set after the last byte of the Command Phase of a Seek or Recalibrate command is issued for drive 3. Cleared after reading the first byte in the Result Phase of the Sense Interrupt Command for this drive.

D2 Drive 2 Seeking: Same as above for drive 2.

D1 Drive 1 Seeking: Same as above for drive 1.

D0 Drive 0 Seeking: Same as above for drive 0.

13.5.2 Data Register (Read/Write)

This is the location through which all commands, data and status flow between the CPU and the DP8473. During the Command Phase the μP loads the controller's commands into this register based on the Status Register Request for Master and Data Direction bits. The Result Phase transfers the Status Registers and header information to the μP in the same fashion.

Table 13-5. Data Rate and Precompensation Programming Values

D1	D0**	DRVTYP Pin	Data Rate MFM (kb/s)	Normal Precomp* (ns)	Alternate Precomp* (ns)	FGND Pin Enabled	RPM/LC Pin Level
0	0	X	500	125	125	FGND500	High
0	1	0	250	125	250	FGND250	Low
0	1	1	300	125	208	FGND250	Low
1	0	0	250	125	250	FGND250	Low
1	0	1	250	125	250	FGND250	Low
1	1	0	1000	83	83	None	High
1	1	1	1000	83	83	None	Low

* Normal values when PUMP/PREN pin set low; Alternate values when PUMP/PREN pin set high.

** D0 and D1 are data Rate Control Bits.

13.5.3 Drive Control Register (Write Only)

D7 Motor Enable 3: This controls the Motor for drive 3, MTR3. When 0 the output is high, when 1 the output is low. (Note this signal is not output to a pin on 48 pin DIP version.)

D6 Motor Enable 2: Same function as D7 except for drive 2's motor. (Note this signal is not brought out to a pin on DIP.)

D5 Motor Enable 1: This bit controls the Motor for drive 1's motor. When this bit is 0 the MTR1 output is high.

D4 Motor Enable 0: Same as D5 except for drive 0's motor.

D3 DMA Enable: When set to a 1 this enables the DRQ, DAK, INT pins. A zero disables these signals.

D2 Reset Controller: This bit when set to a 0 resets the controller, and when a 1 enables normal operation. It does not affect the Drive Control or Data Rate Registers which are reset only by a hardware reset.

D1-D0 Drive Select: These two pins are encoded for the four drive selects, and are gated with the motor enable lines, so that only one drive is selected when it's Motor Enable is active. (See Table 13-4).

13.5.4 Data Rate Register (Write Only)

D7-D2: Not used.

D1, D0 Data Rate Select: These bits set the data rate and the write precompensation values for the disk controller. After a hardware reset these bits are set to 10 (250 kb/s). They are encoded as shown in Table 13-5.

13.5.5 Disk Changed Register (Read Only)

D7 Disk Changed: This bit is the latched complement of the Disk Changed input pin. If the DSKCHG input is low this bit is high.

D6-D0: These bits are reserved for use by the hard disk controller, thus during a read of this register, these bits are TRI-STATE.

13.6 RESULT PHASE STATUS REGISTERS

The Result Phase of a command contains bytes that hold status information. The format of these bytes are described below. Do not confuse these register bytes with the Main Status Register which is a read only register that is always available. The Result Phase status registers are read from the Data Register only during the Result Phase.

13.6.1 Status Register 0 (ST0)

D7-D6 Interrupt Code:
00 = Normal Termination of Command.
01 = Abnormal Termination of Command. Execution of Command was started, but was not successfully completed.
10 = Invalid Command Issue. Command Issued was not recognized as a valid command.
11 = Ready changed state during the polling mode.

D5 Seek End: Seek or Recalibrate Command completed by the Controller. (Used during Sense Interrupt command.)

D4 Equipment Check: After a Recalibrate Command, Track 0 signal failed to occur. (Used during Sense Interrupt command.)

D3 Not Used: 0

D2 Head Address (at end of Execution Phase).

D1, D0 Drive Select (at end of Execution Phase).
00 = Drive 0 selected. 01 = Drive 1 selected.
10 = Drive 2 selected. 11 = Drive 3 selected.

13.6.2 Status Register 1 (ST1)

D7 End of Track: Controller transferred the last byte of the last sector without the TC pin becoming active. The last sector is the End Of Track sector number programmed in the Command Phase.

D6 Not Used: 0

D5 CRC Error: If this bit is set and bit 5 of ST2 is clear, then there was a CRC error in the Address Field of the correct sector. If bit 5 od ST2 is set, then there was a CRC error in the Data Field.

D4 Over Run: Controller was not serviced by the μP soon enough during a data transfer in the Execution Phase.

Table 13-6. Maximum Time Allowed to Service an Interrupt or Acknowledge a DMA Request in Execution Phase

Data Rate	Time to Service
125	62.0μs
250	30.0μs
500	14.0μs
1000	6.0μs

Time from rising edge of DRQ or INT to trailing edge of DAK or RD or WR.

D3 Not Used: 0

D2 No Data: Three possible problems: 1) Controller cannot find the sector specified in the Command Phase during the execution of a Read, Write, or Scan command. An address mark was found however so it is not a blank disk. 2) Controller cannot read any Address Fields without a CRC error during Read ID command. 3) Controller cannot find starting sector during execution of Read A Track command.

D1 Not Writable: Write Protect pin is active when a Write or Format command is issued.

D0 Missing Address Mark: If bit 0 of ST2 is clear then the disk controller cannot detect any Address Field Address Mark after two disk revolutions. If bit 0 of ST2 is set then the disk controller cannot detect the Data Field Address Mark.

13.6.3 Status Register 2 (ST2)

D7 Not Used: 0

D6 Control Mark: Controller tried to read a sector which contained a deleted data address mark during execution of Read Data or Scan commands. Or, if a Read Deleted Data command was executed, a regular address mark was detected.

D5 CRC Error in Data Field: Controller detected a CRC error in the Data Field. Bit 5 o ST1 is also set.

D4 Wrong Track: Only set if desired sector not found, and the track number recorded on any sector of the current track is different from that stored in the Track Register.

D3 Scan Equal Hit: "Equal" condition satisfied during any Scan Command.

D2 Scan Not Satisfied: Controller cannot find a sector on the track which meets the desired condition during Scan Command.

D1 Bad Track: Only set if the desired sector is not found, and the track number recorded on any sector on the track is different from that stored in the Track Register and the recorded track number is FF.

D0 Missing Address Mark in Data Field: Controller cannot find the Data Field Address Mark during Read/Scan command. Bit 0 of ST1 is also set.

13.6.4 Status Register 3 (ST3)

D7 Not Used: 0

D6 Write Protect Status

D5 Not Used: 1

D4 Track 0 Status

D3 Not Used: 0

D2 Head Select Status

D1, D0 Drive Selected:
00 = Drive 0 selected. 01 = Drive 1 selected.
10 = Drive 2 selected. 11 = Drive 3 selected.

13.7 PROCESSOR SOFTWARE INTERFACE

Bytes are transferred to and from the disk controller in different ways for the different phases in a command.

13.7.1 Command Sequence

The disk controller can perform various disk transfer, and head movement commands. Most commands involve three separate phases.

Command Phase: The μP writes a series of bytes to the Data Register. These bytes indicate the command desired and the particular parameters required for the command. All the bytes must be written in the order specified in the Command Description Table. The Execution Phase starts immediately after the last byte in the Command Phase is written. Prior to performing the Command Phase, the Drive Control and Data Rate Registers should be set.

Execution Phase: The disk controller performs the desired command. Some commands require the μP to read or write data to or from the Data Register during this time. Reading data from a disk is an example of this.

Result Phase: The μP reads a series of bytes from the data register. These bytes indicate whether the command executed properly and other pertinent information. The bytes are read in the order specified in the Command Description Table.

A new command may be initiated by writing the Command Phase bytes after the last bytes required from the Result Phase have been read. If the next command requires selecting a different drive or changing the data rate the Drive Control and Data Rate Registers should be updated. If the command is the last command, then the software should deselect the drive. (*Note as a general rule the operation of the controller core is independent of how the μP updates the Drive Control and Data Rate Registers. The software must ensure that manipulation of these registers is coordinated with the controller operation.*)

During the Command Phase and the Result Phase, bytes are transferred to and from the Data Register. The Main Status Register is monitored by the software to determine when a data transfer can take place. Bit 6 of the Main Status Register must be clear and bit 7 must be set before a byte can be written to the Data Register during the Command Phase. Bits 6 and 7 of the Main Status Register must both be set before a byte can be read from the Data Register during the Result Phase.

If there is information to be transferred during the Execution Phase, there are three methods that can be used. The DMA mode is used if the system has a DMA controller. This allows the μP to do other things during the Execution Phase data transfer. If DMA is not used, an interrupt can be issued for each byte transferred during the Execution Phase. If interrupts are not used, the Main Status Register can be polled to indicate when a byte transfer is required.

13.7.2 DMA Mode

If the DMA mode is selected, a DMA request will be generated in the Execution Phase when each byte is ready to be transferred. To enable DMA operations during the Execution Phase, the DMA mode bit in the Specify Command must be enabled, and the DMA signals must be enabled in the Drive Control Register. The DMA controller should respond to the DMA request with a DMA acknowledge and a read or write strobe. The DMA request will be cleared by the active edge of the DMA acknowledge. After the last byte is transferred, an interrupt is generated, indicating the beginning of the Result Phase. During DMA operations the Chip Select input must be held high. TC is asserted to terminate an operation. Due to the internal gating TC is only recognized when the DAK input is low.

13.7.3 Interrupt Mode

If the non-DMA mode is selected, an interrupt will be generated in the Execution Phase when each byte is ready to be transferred. The Main Status Register should be read to verify that the interrupt is for a data transfer. Bits 5 and 7 of the Main Status Register will be set. The interrupt will be cleared when the byte is transferred to or from the Data Register. The μP should transfer the byte within the time alloted by Table 13-6. If the byte is not transferred within the time allotted, an Overrun Error will be indicated in the Reset Phase when the command terminates at the end of the current sector.

An interrupt will also be generated after the last byte is transferred. This indicates the beginning of the Reset Phase. Bits 7 and 6 of the Main Status Register will be set and bit 5 will be clear. This interrupt will be cleared by reading the first byte in the Result Phase.

13.7.4 Software Polling

If the non-DMA mode is selected and interrupts are not suitable, the μP can poll the Main Status Register during the Execution Phase to determine when a byte is ready to be transferred. In the non-DMA mode, bit 7 of the Main Status Register reflects the state of the interrupt pin. Otherwise, the data transfer is similar to the Interrupt Mode described above.

14

POWER SUPPLY

14.1 OVERVIEW

The POWER SUPPLY provides power every board installed in Main Board, Floppy Disk Drive, Hard Disk Drive and the Keyboard. It also provides power for the monitor through its outlet. This chapter describes the performance characteristics of a 275 Watts, 4 outputs level switching mode power supply.

14.2 FUNCTIONAL DESCRIPTION

14.2.1 Input Requirements

The power supply can operate at a frequency of either 50+/−3Hz or 60+/−3Hz and it can operate at 90V AC to 132V AC or 180V AC or 264V AC signal phase. Input current will be less than 5.0 Ampares at full load output condition an minimum voltage.

14.2.2 Output Characteristics

DC Output

Output Voltage	Wire Color	Tolerance (Accuracy)	Load Current Minimum-Maximum
+5 Vdc	RED	+/−3%	5.0 Adc ~ 30 Adc
+12 Vdc	YELLOW	+/−5%	0.5 Adc ~ 10.0 Adc (surge: 14.0 Vdc)
−12 Vdc	BLUE	+/−9%	0 Adc ~ 0.5 Adc
−5 Vdc	GREEN	+/−9%	0 Adc ~ 0.5 Adc
+5 Vdc	ORANGE	+/−5%	POWER GOOD (OPTION)

Note: The wire color of GND line is BLACK.

AC Output

Output Voltage	Tolerance (Accuracy)	Load Current Minimum-Maximum
115 Vac	90 Vac ~ 132 Vac	0 Aac ~ 5.0 Aac
230 Vac	180 Vac ~ 264 Vac	0 Aac ~ 2.5 Aac

14.2.3 Voltage Adjustment

The +5V DC output will be adjustable from 4.75V DC to 5.25V DC. The +5 volts output at the power supply output connector should be adjusted to between 4.9 volts to 5.1 volts by the manufacturer for typical load operation.

14.2.4 Over Voltage Protection

This protection is effective on the +5V DC and +12V DC outputs. If an overvoltage fault occurs (internal to the power supply), the power supply shall shutdown before +5V DC and +12V DC output exceeds 130% of its nominal value.

14.3 PIN ASSIGNMENTS

Disk Drive Connector

Pin #	Connector #	Voltage (V DC)
1	P5 ~ P8	+12V DC
2, 3		GND
4		+5V DC
1	P4	+5V DC
2, 3		GND
4		+12V DC

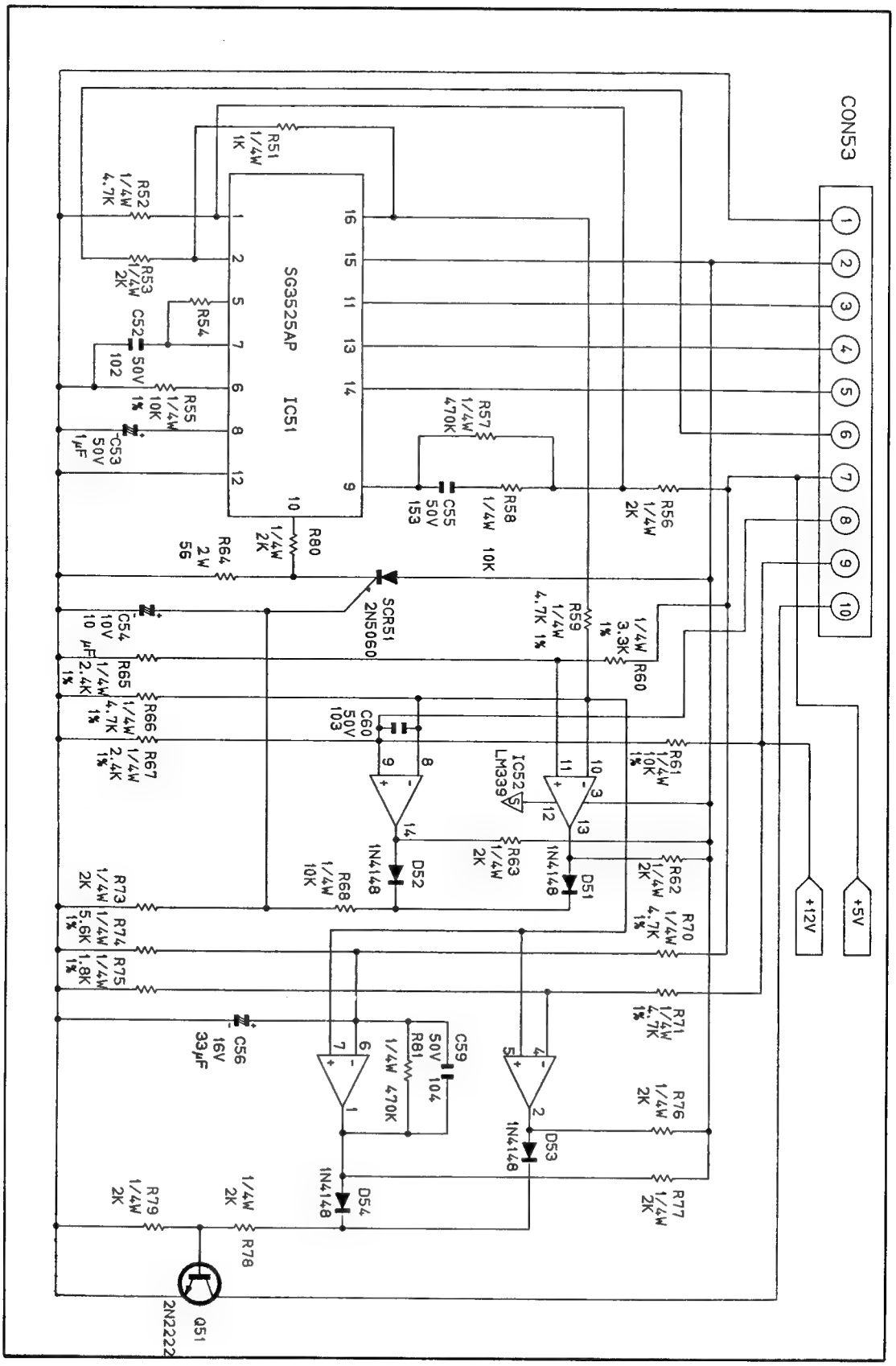
DC Fan Connector

Pin #	Connector #	Voltage (V DC)
1	P9	+12V DC
2		GND

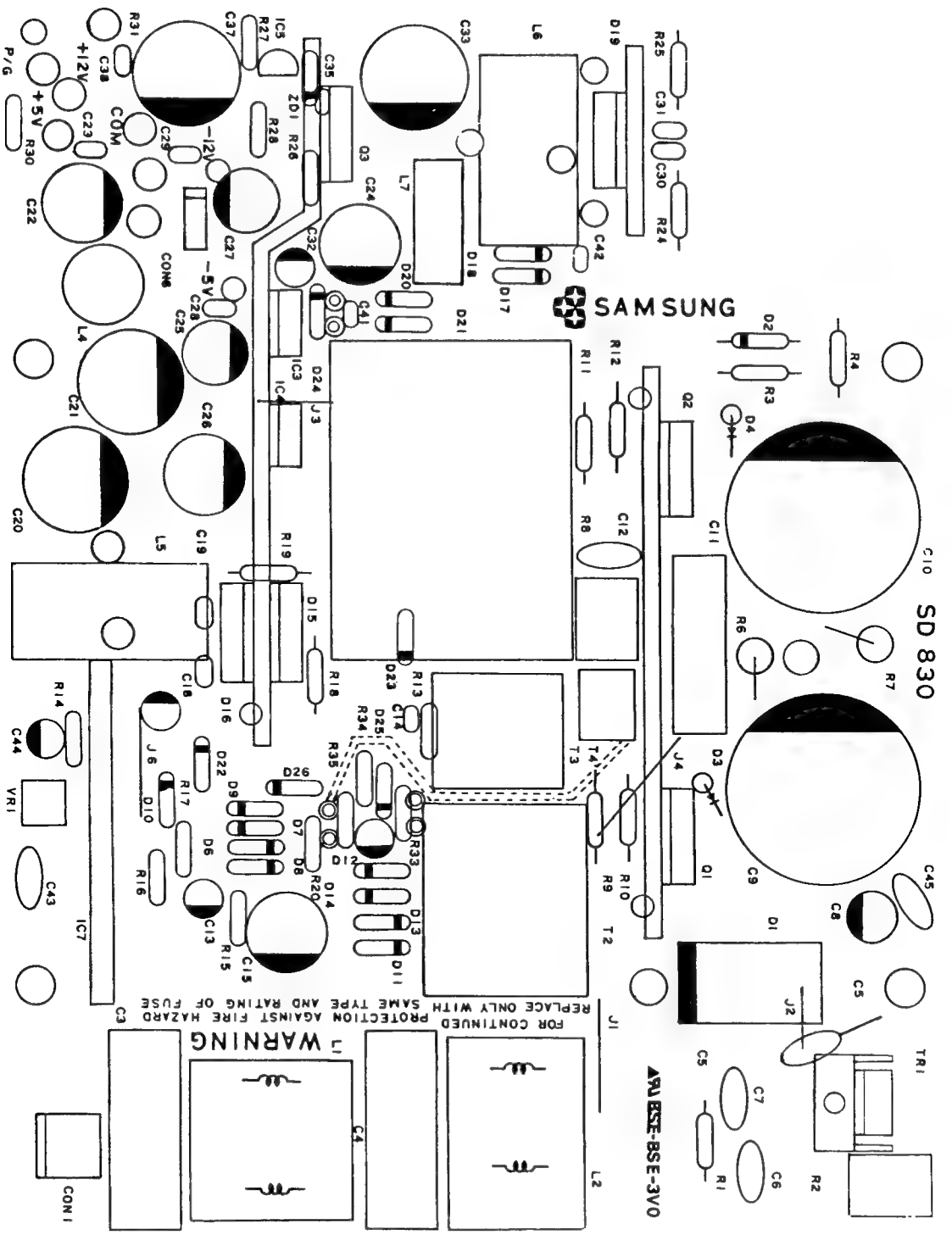
System Power Connector

Pin #	Connector #	Voltage (V DC)	
	1		POWER GOOD (Option)
	2		GND
	3		+12V DC
	4	P1~P3	−12V DC
	5-8		GND
	9		−5V DC
	10-12		+5V DC

14.4 POWER SUPPLY CIRCUIT



14.5 PS-27 SMPS COMPONENTS LAYOUT



14.6 SWITCHING POWER SUPPLY (PS-27) PARTS LIST

Location No	Description	Specification	Unit	Q'ty	Vender
R15, 20, 33, 51, 64	R-METAL FILM	RD 1/4T 1K-J	EA	5	ABCO
R75	R-METAL FILM	RD 1/4T 1.8K-F	EA	1	ABCO
R27, 31, 55, 58, 61	R-METAL FILM	RD 1/4T 10K-F	EA	5	ABCO
R54	R-METAL FILM	RD 1/4T 240-J	EA	1	ABCO
R53, 56, 62, 63, 68	R-METAL FILM	RD 1/4T 2K-J	EA	5	ABCO
R73, 76, 77, 78, 79	R-METAL FILM	RD 1/4T 2K-J	EA	5	ABCO
R65, 67	R-METAL FILM	RD 1/4T 2.4K-F	EA	2	ABCO
R28, 32	R-METAL FILM	RD 1/4T 2.59K-F	EA	2	ABCO
R17, 34	R-METAL FILM	RD 1/4T 24K-F	EA	2	ABCO
R16	R-METAL FILM	RD 1/4T 3K-F	EA	1	ABCO
R60	R-METAL FILM	RD 1/4T 3.3K-F	EA	1	ABCO
R35	R-METAL FILM	RD 1/4T 3.6K-F	EA	1	ABCO
R14	R-METAL FILM	RD 1/4T 4.7-J	EA	1	ABCO
R30	R-METAL FILM	RD 1/4T 470-J	EA	1	ABCO
R59, 66, 70, 71	R-METAL FILM	RD 1/4T 4.7K-F	EA	4	ABCO
R26, 52	R-METAL FILM	RD 1/4T 4.7K-F	EA	2	ABCO
R57, 81	R-METAL FILM	RD 1/4T 470K-F	EA	2	ABCO
R80	R-METAL FILM	RD 1/4T 56-J	EA	1	ABCO
R74	R-METAL FILM	RD 1/4T 5.6K-F	EA	1	ABCO
R13	R-METAL FILM	RD 1/4T 680-J	EA	1	ABCO
R1	R-METAL FILM	RD 1/2T 390K-J	EA	1	ABCO
R18, 19, 21, 22	R-METAL OXIDE	RD 1W 10-J	EA	4	ABCO
R24, 25	R-METAL OXIDE	RD 1W 10-J	EA	2	ABCO
R9, 11	R-METAL OXIDE	RD 1W 33-J	EA	2	ABCO
R10, 12	R-METAL OXIDE	RD 1W 470-J	EA	2	ABCO
R3, 4	R-METAL OXIDE	RD 1W 100-J	EA	2	ABCO
R6, 7	R-METAL OXIDE	RD 2W 47K-J	EA	2	ABCO
R2	R-CEMENT	RD 5W 10-J	EA	1	ABCO
R8	R-CEMENT	RD 5W 220-J	EA	1	ABCO
VR1	VR-SEMI	3323S 1/2W 1K	EA	1	COPAL
C18, 19, 30, 31, 41	C-CERAMIC	HCYB3A102K 1KV 102	EA	5	SEMCO
C42	C-CERAMIC	HCYB3A102K 1KV 102	EA	1	SEMCO
C12	C-CERAMIC	HCYB3D561K 2KV 561	EA	1	SEMCO
C23, 28, 29, 38	C-CERAMIC	CCYV1H104Z 50V 104	EA	4	SEMCO
C5, 6, 7, 43	C-CERAMIC	HCYF2E472M 250V 472-Y	EA	4	SEMCO
C45	C-CERAMIC	HCYF2E222M 250V 222-Y	EA	1	SEMCO
C60	C-CERAMIC	CCYF1H103Z 50V 103	EA	1	SEMCO
C35	C-MONO, CERAMIC	50V 103	EA	1	CENTRAB
C11	C-POLYESTER	250V AC 2.2uF	EA	1	SHINSHIN
C14, 52	C-POLYESTER	50V 102	EA	2	DONGKUCK
C59	C-POLYESTER	100V 104	EA	1	DONGKUCK
C55	C-POLYESTER	100V 153	EA	1	DONGKUCK
C57	C-POLYESTER	100V 222	EA	1	DONGKUCK
C3, 4	C-POLYPROPYLENE	XG-V 275V 474-X	EA	2	TEAPO
C58	C-POLYPROPYLENE	XG-V 275V 224-X	EA	1	TEAPO
C53	C-ELECTROLYTIC	CEGLX1H010 50V 1uF	EA	1	SEMCO
C13, 32, 39, 40, 44	C-ELECTROLYTIC	CEGLX1H4R7 50V 4.7uF	EA	5	SEMCO
C56	C-ELECTROLYTIC	CEGLX1C330 16V 33uF	EA	1	SEMCO
C8	C-ELECTROLYTIC	CEGLX1V470 35V 47uF	EA	1	SEMCO
C54	C-ELECTROLYTIC	CEGLX1A101 10V 100uF	EA	1	SEMCO
C25, 27	C-ELECTROLYTIC	CEGLT1C221 16V 220uF	EA	2	SEMCO
C26	C-ELECTROLYTIC	CEGLT1C471 16V 470uF	EA	1	SEMCO
C24	C-ELECTROLYTIC	CEGLT1E471 25V 470uF	EA	1	SEMCO
C9, 10	C-ELECTROLYTIC	CESMS2D681 200V 680uF	EA	2	SEMCO

APPENDIX

A. DIAGNOSTIC
B. MESSAGES
C. SCHIMETIC
D. PART LIST
E. EXPLODED VIEW

A

DIAGNOSTIC

A.1 DIAGNOSTIC PROGRAM OVERVIEW

There are six files for diagnostic program.

LOADER.COM
DIAG.EXE
VGA.EXE
KEYIN.DAT
HELP.DAT
ERROR.REC

1. LOADER.COM loads DIAG.EXE (main program) and runs it.
2. DIAG.EXE is a main program.
3. VGA.EXE is a EGA/VGA test program.
4. KEYIN.DAT has the information of the Auto-Test procedure.
5. HELP.DAT contains Help-Messages.
6. ERROR.REC contains Error informations during Test.

* This diagnostic program runs in DOS environment (Version 3.x, Above)

A.2 HOW TO BOOT THIS DIAGNOSTICS PROGRAM

A.2.1 Run Diagnostics

Just type "LOADER" (if EGA/VGA Adapter is installed tyte "LOADER VGA.EXE") and press <Enter> key.

Next time you can see following message on center of screen.

```
Serial Number: 1990 - 0101 - 0001
Press <Enter> to continue ....
```

A.2.2 Serial Number

1. Serial number is used to identify the system on testing.
2. If you don't want to edit "Serial Number" just press <Enter>.
3. If you want to edit you can use <Cursor> / <Numeric> key.
4. Edited Serial-Number will be saved on diskette.

A.2.3 Caution

1. Now you can see following messages.

> **≪Notice for successful testing≫**
>
> a) All diskette must be formatted by this program for FDD R/W test otherwise R/W test will be Skipped.
>
> b) During HDD R/W Test all data will be saved.
>
> Press <Enter> to continue ....

2. Diskette requirements.
   a) For FDD R/W test all diskette should be formatted by this program.
   b) If you want format with option /S (system transfer), first format target diskette by this program next transfer SYSTEM by SYS.COM and then copy COMMAND.COM on target diskette.

A.2.4 Press <F9> key to display System Configuration and press <F9> again for HELP message

A.2.5 Press <Enter> key to continue.

A.3 DESCRIPTION OF SCREEN & FUNCTION KEY USAGE

A.3.1 Followings are disagnostics' MAIN MENU

AT System Diagnostics Version 2.00X Copyright (C) SAMSUNG Electronics Co., Ltd. 1990.	Current Time: 12:15:28 Elapsed Time: 03:39:21

Manual | Automatic | Auto Edit | Def. Auto | Init. | Disp Err. | Aging Off | Exit

In [Manual] mode you can test every function manually
MENU system has a hierachical structure

	Pass	Fail
System Board		
Keyboard		
Video Adapter		
Floppy Disk.		
Fixed Disk.		
Parallel Port.		
Serial Port.		

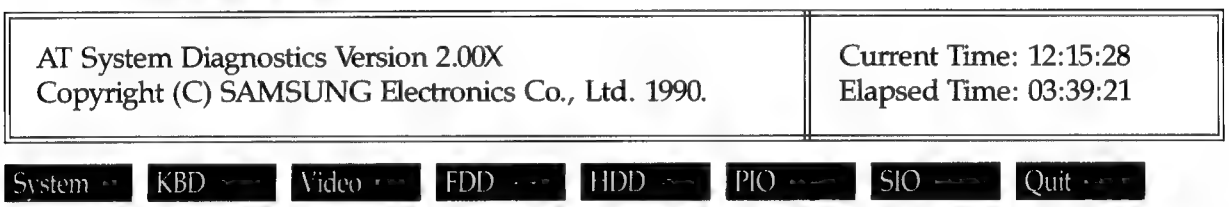
A.3.2 How to Select Each MENU

The MENU has a hierachical structure.

1. At first CURSOR is located at Manual position.
2. Now you can move this CURSOR position by using <CURSOR LEFT/RIGHT> keys.
3. To enter SUB MENU press <Enter> key or ®CURSOR DOWN> key.
4. And also you can enter SUB MENU directly by pressing corresponding function key <F1>-<F8>.
5. To return previous MENU press <Esc> key or <CURSOR UP> Key. Select Quit brings same effect.

A.4 DESCRIPTION OF MANUAL TEST MODE

If you select **Manual** on MAIN MENU you can see next screen.



In this mode you can test every function manually.

If error detected during test, error message will be displayed on screen.

If you want to save this eror status press <Y>
If don't want, press <N> or <Esc> key.

A.4.1 System Menu

1. **BIOS ROM** : It tests Checksum of System BIOS ROM (F000:0000 - FFFF) and Additional System Board ROM (E000:0000 - FFFF).

2. **I/O ROM** : It tests Checksum of I/O Adapter's ROM which is valid and test range is (C000:0 - D000:FFFF).

3. **RAM** : It performs R/W test of SYSTEM Accessible R/W Memory. It's test range is Base 640KB and Extend Memory up to 16MB.

4. CMOS RAM : It tests CMOS RAM (10H - 3FH) and save original value.

5. Speaker : It tests speaker tone.

   : Numeric key (<1> - <8>) will sounds 'Do' - 'Do'. with corresponding frequency displayed.

   Freq + : Increases current frequency by 10Hz at every stroke.

   Freq − : Decreases current frequency by 10Hz at every stroke.

6. Quit : Returns back to MAIN MENU.

A.4.2 KBD Menu

1. Reset KBD : Sends RESET COMMAND to Keyboard Processor and waits completion code from Keyboard Processor.

2. Scan Code : It tests Make/Break Code of every key.
   This test cannot be terminated w/o User key input.

3. Quit : Returns back to MAIN MENU.

A.4.3 Video Menu

1. Mode Test : It tests all Modes and functions on current Video Adapter.
   Note) If EGA monitor is attached to VGA adapter then it tests only possible display mode on EGA monitor.

2. Chip Diag : It tests EGA/VGA registers, Video RAM and external palette RAM. It also tests Read mode 0/1, Write mode 0/1/2 whether it works correctly or not.

A.4.4 FDD Menu

1. FDD Reset : Reset FDD system.
   On Manual operation it also does FDD surface scanning.

2. Format : Format diskette.
   You must select diskette type as correctly.
   Formatted diskette can be used like the one of DOS Format.
   But in this format R/W region will be reserved on diskette it occupies ONE-start, TWO-middle, One-last of Track (each side).
   So EIGHT will be appeared in FAT area.

3. R/W Test : It tests R/W function of Drive not Media.
   If R/W error detected that sector is marked as BAD for not to test in next time. This avoid the propagation of media error to drive error.

4. Seeking : Performs Ramdom and Seqntial seek test.

5. Motor Spd : Checks the rotation speed of Spindle Motor at 10 times.
   Estimated speed will be displayed in msec unit with maximum and minimum value.

6. Quit : Returns back to MAIN MENU.

A.4.5 HDD Menu

1. HDD Reset : Performs HDD controller internal diagnostics.

2. Format : Low level format of HDD (At standard)
   You can give factory BAD track map and interleave mode.

3. R/W Test : Performs R/W test with original data saved.
   On AGING ON mode whole track will be tested but on AGING OFF mode not whole.

4. Seeking : Performs Random and Seqntial seek test.

5. Quit : Returns back to MAIN MENU.

A.4.6 PIO Menu

1. Before test loopback connector is to be installed in PIO port. Refer to HELP for Loopback connection.

2. It performs internal data loop back test, external control signal and Interrupt generation and dectection.

A.4.7 SIO Menu

1. Like PIO test loopback should be installed properly.

2. Manual mode.

   Select COM # and Internal / External loopback mode.
   Then it tests all combination of Parity/Data bits/Stop Bits at 2400 baudrate.

3. Auto mode

   This mode tests whole installed port, Internal / External mode, all combination of Parity/Data bits/Stop Bits at 9600/1200/150 baudrate.

4. Quit : Returns back to MAIN MENU.

A.5 DESVRIPTION OF AUTO TEST MODE

If you select Automatic on MAIN MENU following text will be displayed.

AT System Diagnostics Version 2.00X Copyright (C) SAMSUNG Electronics Co., Ltd. 1990.	Current Time: 12:15:28 Elapsed Time: 03:39:21

Whole | Memory | Diskette | Hard Disk | Video | Speaker | User Def. | Quit

	Pass	Fail
System Board		
Keyboard		
Video Adapter		
Floppy Disk.		
Fixed Disk.		
Parallel Port.		
Serial Port.		

In this mode, the test is performed continuously w/o key input.
Its test procedure is stored in KEYIN.DAT file.

A.5.1 Description of Each Test Procedure

1. Whole test

   This test diagnoses whole systems.
   In this test other Auto tests (Memory , Video , Diskette , Hard Disk and Speaker) is invoked as sub procedure.

2. Memory test

   This performs test of BIOS ROM, Additional System ROM, I/O Adapter ROM, Base/Extended RAM and CMOS RAM.
   And above is repeated.

3. Diskette test

   It tests floppy disk driver according to System configuration.
   Test items are FDD Reset , R/W Test , Seeking and Motor Spd .
   And repeats them continuously.

4. Hard Disk test

   It tests fixed disk driver according to System configuration.
   Test items are HDD Reset , R/W Test and Seeking .
   And above is repeated.

5. Video test

   a) Default Mode case (w/o VGA.EXE option when booting Diagnostics)

      Test items are Text Mode , Graphic , Alignment and Video RAM .
      And repeates them continuously.

   b) EGA/VGA test Mode

      Test items are Mode Test and Chip Diag .
      And repeates them.

6. Speaker test

   It sounds Do, Re, Mi, Fa,.... Mi, Re, Do and frequency increases upto 1112Hz.
   And repeates above.

7. User Def. test

   His procedure can be defined by User.

8. Quit : Returns back to MAIN MENU.

A.5.2 How it Works?

1. Once Automatic test is started it does not stop unless Press <Ĉ> key. When test procedure comes to end, it is wrap around to start and repeated from start.

2. If an automatic procedure contains Sub-Automatic test procedure, the Sub procedure (Inner Auto procedure) will be performed by on time. And the Main procedure (Outer Auto procedure) is continued. When Main procedure meet End of test it is repeated from the Start. So Sub procedure will be invoked again.

3. Currently Whole test procedure invokes other Auto procedure and invoked procedure does not contain another Auto procedure. But this program allows one more Sub-Auto procedure to be invoked.

4. KEYIN.DAT file contains definition of each Auto-test procedure. This file is initialized automatically if there is no KEYIN.DAT file in current directory.
   And it also be initialized at any time by Init. Menu.
   When KEYIN.DAT is initialized each test procedure is adjusted properly according to current System Configuration.

A.6 DESCRIPTION OF AUTOMATIC PROCEDURE EDITOR

If you select **Auto Edit** to MAIN MENU the following text will be displayed.

Automatic Test Procedure Screen Editor Copyright (C) SAMSUNG Electronics Co., Ltd. 1990.	Current Time: 12:15:28 Elapsed Time: 03:39:21

(Automatic Test Procedure LABEL will be displayed)

Welcome! Select Auto-Test Procedure you want to edit ...

1 Whole 2 Memory 3 Diskette 4 Hard Disk 5 Video 6 Speaker 7 User Def. 8 Quit

A.6.1 If you select **Diskette** following text will be displayed.

Automatic Test Procedure Screen Editor Copyright (C) SAMSUNG Electronics Co., Ltd. 1990.	Current Time: 12:15:28 Elapsed Time: 03:39:21

Manual FDD FDD Reset Drv A: Quit Seeking Drv A: Seqntial

Drv A: Random Quit Motor Spd Drv A: Quit R/W Test Drv A:

Quit [Del] FDD Reset Drv B: Quit Seeking Drv B: Seqntial

Drv B: Random Quit Motor Spd Drv B: Quit R/W Test Drv B:

Quit [End]

Control Keys	[Ins] [Del] [↑↓←→] [Esc] / [Space] [Enter] - Select Item to Edit

CURSOR is located **Manual** which atributte is some different than other's.
And now you are in [Ins] / [Del] Mode.
In this mode you can delete or insert test procedure by using]Ins] / [Del] key.

1. Delete procedure: Move CURSOR to position you want to delete, and press [Del] key.

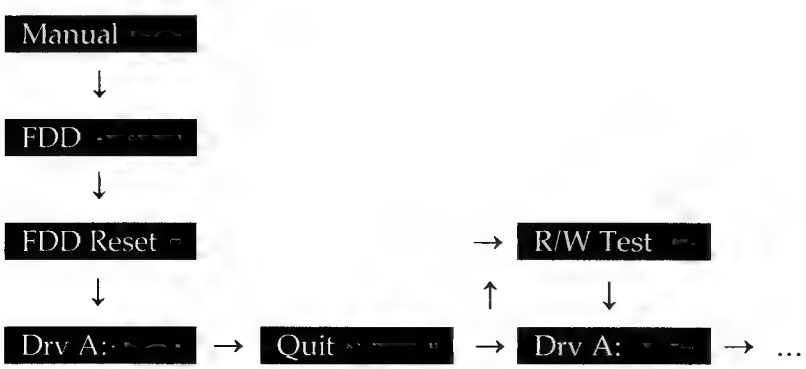
   * **Notice:** When you delete one LABEL you can see following procedure (LABEL's Name) is changed strangely.

     The reason is as below.

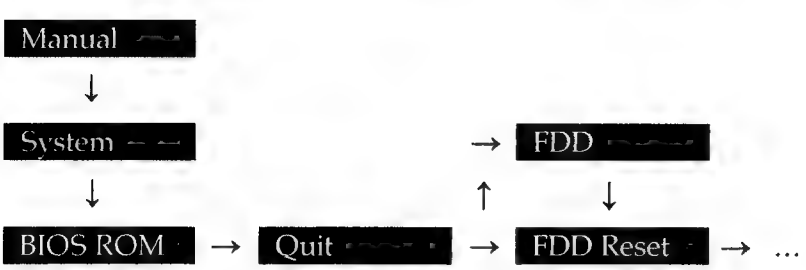
   a) The Structure of Auto-Test procedure:

   The procedure is defined as streams of "scan code". (Actual value is <F1> = BBH .... <F8> = C2H.)

   In case of Diskette , the actual code sequence is <F4> - <F1> - <F1> - <F8> - <F3> - <F1> - ... which corresponds to diagram below.



   if you delete FDD only, test procedure will be as follow.



   b) So if you are to delete a test module you must delete upto Quit LABEL.

2. Insert procedure: Move CURSOR to position you want to insert, and press [Ins] key then undefined procedure like <?> will be inserted. Now you can define this LABEL as you want.

A.6.2 How to Define <?> , or Change Procedure Already Defined

1. Move CURSOR with <CURSOR KEY> and select item you want to Edit.
2. Press <SPACE BAR>.
3. Then control key menu is changed as following.

Control Keys	[←→] - Select Item / [Space] [Enter] - Change Item / [Esc] - Exit

4. Move CURSOR to position and press <SPACE BAR> / <ENTER> key.
5. Then selected item will be changed.

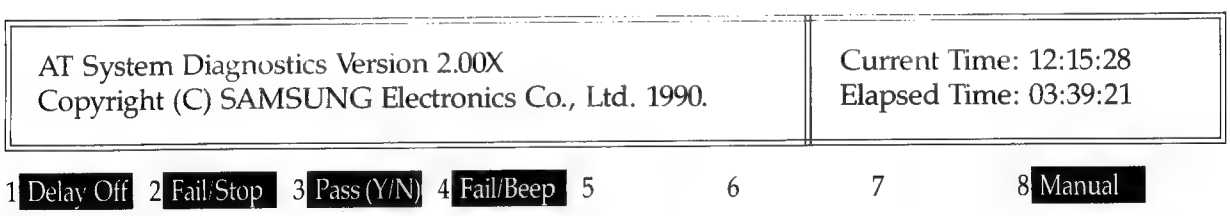
A.6.3 Exit Editor

1. Press <Esc> in]Ins] / [Del] mode.
2. If you want to save press <Y> key.
3. [End] LABEL is usd by system and cannot be deleted.
4. [Del] LABEL is used by system also and can be deleted.
   This LABEL is used for adjust Auto procedure when Diagnostics is booting.
   (for example, Kill Dry B: test procedure when B: is not installed)
   But edited procedure is not adjusted automatically.

A.7 DESCRIPTION OF AUTOMATIC PROCEDURE DEFINE MODE

This mode is used to make new Auto test procedure and is more useful than Auto Edit mode when edit a lot of procedure.

1. First select Auto-test procedure to define.
2. Enter new name of procedure and press <Enter> key.
3. Then following MENU will be shown.



While running Automatic Procedure all time delay loop for Manual Procedure will be passed.

A.7.1 Description of Error Handling Option

1. Delay Off : If selected, during Auto-test all time delay for user will be skipped to save time.
2. Fail/Stop : If selected, this diagnostics waits for user key input on error detection. And asks you to save or not error condition. If not selected, error condition will be saved Automatically into ERROR.REC file.
3. Pass (Y/N) : If not selected, Video test will be passed w/o user key input. If selected, waits for user key input (Y/N). In case of key input is "N" then it assumes error be occurred.
4. Fail/Beep : If selected, it generates 10 times beep sound on error detection.

A.7.2 Manual : Starts to Define Detail Procedure Step by Step

A.7.3 How to Save Defined Procedure?

1. Press <End> key to terminate current job.
2. If you want to save then press <Y> key, then defined procedure will be saved into KEYIN.DAT file.
3. If you don't save, you can use them after Power-Off.

A.8 Init. FUNCTUIN

1. Error Rec : It initializes or creats ERROR.REC file and clear error record in memory.
2. Keyin. dat : It initializes KEYIN.DAT and adjsut according to System Configuration

A.9 Disp Err. FUNCTION

1. It displays error record on screen in following format. (example)

Error No.	Error Code	Description	Date/Time
0001	12 00D4	BIOS ROM Checksum Error	1989 01 04 15:11

1) Error No : Error number.
2) Error Code : 12 – sort of error (BIOS ROM Checksum Error)
   00D4 – detail error condition (refer to HELP)
3) Description : Describes the error briefly.
4) Date/Time : Error occurred time and date.

A.10 Aging Off / Aging On FUNCTION

It is toggled at every selection and updates DIAG.EXE file according to current status.

If current status is Aging On when you re-boot diagnostics it runs Whole procedure w/o key input.

It is useful to start burn-in test by AUTOEXEC.BAT file.

To switch to Aging Off state, press <^C> key and press Aging On on MAIN MENU.

A.11 Exit FUNCTION

Exit to DOS.

A.12 ERROR CODE DESCRIPTION

A.12.1 System [1?]

10 (System RAM) 08 xx
- 10H : High Address Bus Short Error
- 20H : Data Bus Short Error
- 30H : Data Pattern R/W Error
- 31H : Parity Error
- 40H : Even/Odd Bank Access Error
- 50H : Cell Test Data Error
- 51H : Cell Test Address Error

08 0000H – 08 FFFFH (Error block in 64K unit)

11 (Cache SRAM)
- 0800H – 08FFH (Error Page No.)
- xx : Error Bit Set.

12 (BIOS ROM) 002C: byte checksum Error value
13 (Extended BIOS ROM) 002C : byte checksum Error value – socket on CPU board
14 (I/O Card ROM) 002C : byte checksum Error value – EGA Card BIOS & etc.
15 (CMOS RAM R/W Error) 21 04
- 0000 0100 (Error Bit Set)
- Error Address (21H Register)

16 (Speaker Error) 00 00
- No meaning

17 (PMS data line test Error) 00 55 – Error data
18 (PMS back-light test Error)
19 (PMS micro-S/W test Error)
1A (PMS battery charging test Error)

A.12.2 Keyboard [2?]

20 (Keyboard Processor Reset Error) 00 0D – received code other than AAH
21 (Keyboard Scancode test Error) 00 00 – no meaning
22 (Keyboard controller BAT Error)

A.12.3 Video Adapter [3?] (CGA/MGA Case Only)

30 (EGA/VGA general Error)
31 (Video RAM test Error)
32 (Read mode 0 test Error)
33 (Read mode 1 test Error)
34 (Write mode 0 test Error)
35 (Write mode 1 test Error)
36 (Write mode 2 test Error)
37 (Write mode 3 test Error)
38 (Switch setting test Error)
39 (Reading inactive plane test Error)
3A (Reading active plane test Error)
3B (Rotation function test Error)
3C (Linear address test A0-A7 Error)
3D (Linear address test A9-A15 Error)
3E (Cursor address test A0-A7 Error)
3F (Cursor address test A8-A15 Error)
40 (Cursor address test A16-A17 Error)
41 (Bit mask function test Error)
42 (Latched data test Error)
43 (Even/Odd mode test Error)
44 (CRTC/TS/GDC/ATC test Error)
45 (Internal REG test Error)
46 (Ext palette short test Error)
47 (Ext palette R/W test Error)
48 (Translation ROM data test Error)
49 (EGA/VGA Chip diagnostics Error)
50 (Color Attribute test Error)
51 (Character set test Error)
52 (80X25 mode test Error)
53 40X25 mode test Error)
54 (80X60 mode test Error)
55 (320X200 palette 0 test Error)
56 (320X200 palette 1 test Error)
57 (640X200 2 color test Error)
58 (640X200 16 color test Error)
59 (640X350 16 color test Error)
5A (640X480 16 color test Error)
5B (800X600 16 color test Error)
5C (1024X768 16 color test Error)
5D (320X200 256 color test Error)
5E (640X480 256 coloor test Error)
5F (8 page change test Error)
60 (Text scrolling test Error)
61 (2 font display test Error)
62 (8 font display test Error)

63 (Panning/Split screen test Error)
64 (Smooth scroll test Error)
65 (Window/Zoomming test Error)
66 (100X50 16 color test Error)
67 (720×512 16 color test Error)
68 (Video display test Error)
69 (Vga. exe Load & Exec Error)

A.12.4 Floppy Disk [7?]

70 (Reset Error)
71 (Format Error)

d0 00 ——————d : Error Drive (0 / 1)
00 00 ——————no meaning)

72 (R/W Test Error)

xx xx
h00s ssss s : Error Sector (1 - 12H)
h : Error Head (0 / 1)
dttt tttt t : Error Track (0 - 4FH)
d : Error Drive (0 / 1)

73 (Seeking Error)

d0 tt ——————tt : Error Track (0 - 4FH)
——————d : Error Drive (0 / 1)

74 (Motor Speed Error)

d1 96 ——————196 : Time for one rotation (μs)
——————d : Error Drive (0 / 1)

A.12.5 Fixed Disk [8?]

80 (Reset Error)
81 (Format Error)

d000 0000 0000 0000 ——d : Error Drive (0 / 1)
dhhh h0tt tttt tttt
——t : Error Track (0 - 1023)
——h : Error Head (0 - 15)
——d : Error Drive (0 / 1)

82 (R/W Test Error) ——— same as Format
83 (Seeking Error)

d000 00tt tttt tttt —— t : Error Track (0 - 1023)
—— d : Error Drive (0 / 1)

84 (HDD ECC Error)

A.12.6 Printer Port Test [9?]

90 Data Port R/W Error
Op xx (same as below)

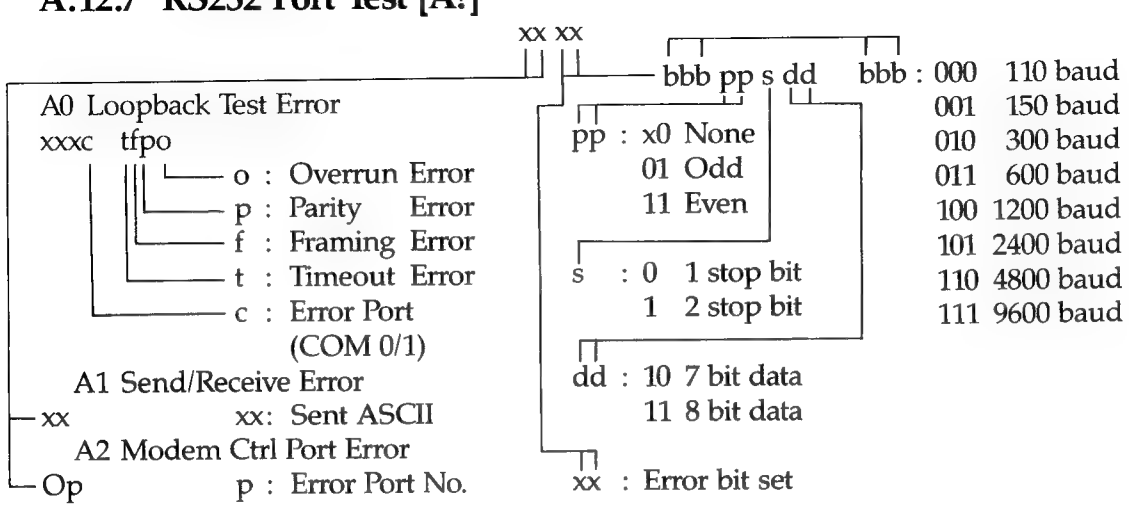
91 Control Port R/W Error
Op xx
- Error Bit Set
- Error Port# (LPT 0/1)

92 Loop-Back Test Error
Op xx
- 0 0 0 1 1 1 1 1 Error Pin Combination
  - (02)—(15)
  - (01)—(13)
  - (12)—(14)
  - (10)—(16)
  - (11)—(17)
- Error Port# (LPT 0/1)

93 Interrupt Test Error
Op xx
- No meaning
- Error Port# (LPT 0/1)

94 Printing test Error

A.12.7 RS232 Port Test [A?]



A3 RxD INT Test Error
A4 TxD INT Test Error
A5 Break INT Test Error
A6 DCD/CTS INT Test Error
A7 DSR/RI INT Test Error
A8 Overrun INT Test Error

Op xx
- no meaning
- Error Port# (COM 1/2)

A9 Baud Test Error Op xx
- no meaning
- Error Port# (COM 1/2)

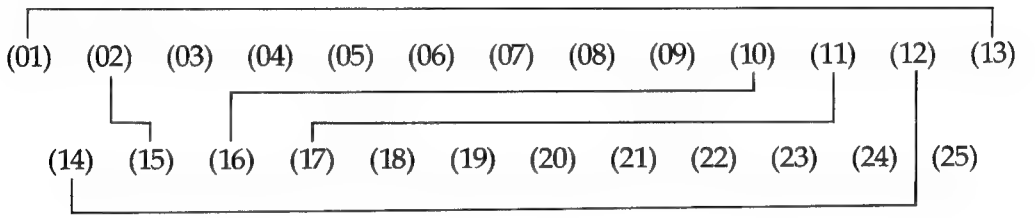
AA Port not attached Error
AB loopback test timeout Error
AC INT test timeout Error

A.12.9 Ethernet Test [C?]

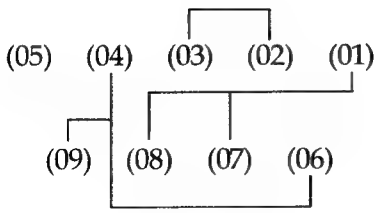
B0 NIC I/O Port not found Error
B1 No Shared RAM found Error
B2 RAM test Error: 0000 test #1
B3 RAM test Error: FFFFtest #2
B4 RAM test Error: A55Atest #3
B5 RAM test Error: inc test #4
B6 RAM test Error: 0000 test #5
B7 Transmit has hung Error
B8 Receive has hung Error
B9 NIC Loopback test Error
BA SNI Loopback test Error
BB CRC mismatch Error
BC CABLE not testminated Error
BD CTI Loopback test Error
BE IRQ test Error

A.13 LOOPBACK PIN CONFIGURATION

[Printer Port Test]



[RS232 Port Test]



B

MESSAGES

B.1 INTRODUCTION

This chapter describes the various system screen messages and error beep codes. Information is grouped as follows:

- POST and boot error messages
- POST and boot informational messages
- Run-time messages
- System board errors
- Beep codes for fatal errors
- Beep codes for non-fatal errors

B.2 POST AND BOOT MESSAGES

The POST displays messages to indicate errors in hardware, software, or firmware, or to provide other information.

If the POST can display a message on the video display screen, it will beep the speaker twice as the message appears. However, when an error occurs before the video display is initialized, the POST cannot display messages on the screen. POST sounds a series of beeps instead.

The next three sections provide a general grouping of messages, with each group arranged in alphabetical order. Each message is accompanied by a short paragraph describing the message and a recommended solution to the problem.

Italics indicate variable parts of a message such as memory addresses. These variable parts at the message may differ at each occurrence.

B.2.1 Post and Boot Error Messages

Message	CACHE memory failure - Disabling. CACHE - Strike the F1 key to continue, F2 to run the Setup utility.
Possible Cause	The cache memory is defective.
Solution	Contact your service representative.
Message	Diskette drive 0 seek failure.
Possible Cause	Drive A has either failed or is missing.
Solution	Check that drive A is present and the floppy disk is inserted properly. Most importantly, check that the cables are installed correctly. If the drive, floppy, disk, and cables appear to be satisfactory, then drive A may have failed. If the problem persists, contact your service representative.
Message	Diskette drive 1 seek failure.
Possible Cause	Drive B has either failed or is missing.
Solution	Check that drive B is present and the floppy disk is inserted properly. Most importantly, check that the cables are installed correctly. If the drive, floppy disk, and cables appear to be satisfactory, then drive B may have failed. If the problem persists, contact your service representative.
Message	Diskette read failure - strike F1 to retry boot. F2 for Setup utility.
Possible Cause	A nonbootable or defective floppy disk, or the drive heads may need cleaning.
Solution	Replace the floppy disk with a bootable floppy disk or another copy and try again. Clean the floppy disk drive heads, in necessary.
Message	Diskette subsystem reset failed.
Possible Cause	The floppy disk drive control cable has failed.
Solution	Check the floppy disk drive control cable. If the problem persists, contact your service representative.
Message	Display adapter failed; using alternate.
Possible Cause	The monitor type jumper is set incorrectly or the primary monitor controller has failed.

Solution	Check to ensure that the monitor type jumper is set correctly. Check the primary monitor controller. If the problem persists, contact your service representative.
Message	Gate A20 failure.
Possible Cause	The computer cannot switch into protected mode.
Solution	Contact your service representative.
Message	Hard disk configuration error.
Possible Cause	The specified configuration is incorrect.
Solution	Return the Setup program and enter the correct fixed disk drive type number. If the problem persists, contact your service representative.
Message	Hard disk controller failure.
Possible Cause	The drive controller board has failed.
Solution	Check the connections at both ends of the fixed disk control and data cables and reseat the drive controller. If the problem persists, contact your service representative.
Message	Hard disk failure or Hard disk read failure - strike F1 to retry boot. F2 for Setup utility.
Possible Cause	The fixed disk is defective.
Solution	Check the system configuration and drive type, and return the Setup utility. Check the connections at both ends of the fixed disk control and data cables and reseat the drive controller. Check the fixed disk drive jumper and termination resistor. If the problem persists, contact your service representative.
Message	Hex-value optional ROM bad checksum = hex-value
Possible Cause	A peripheral board contains a defective ROM or its address conflicts with another board.
Solution	Replace the ROM or the peripheral board, or correct the address confict. If the problem persists, contact your service representative.
Message	Invalid configuration information - please run the Setup utility.

Solution — Check the system configuration and return the Setup utility.

Message — Keyboard clock line failure.

Possible Cause — Either the keyboard or the keyboard cable connection is defective.

Solution — Check the keyboard connection. If the connection is good, the keyboard may have failed. Try running the keyboard diagnostic test. If the problem persists, contact your service representative.

Message — Keyboard controller failure.

Possible Cause — The keyboard controller located on the system board has failed.

Solution — Contact your service representative.

Message — Keyboard data line failure.

Possible Cause — Either the keyboard or the keyboard cable connection is defective.

Solution — Check the keyboard connection. If the connection is good, the keyboard may have failed. If the problem persists, connect your service representative.

Message — Keyboard is locked - please unlock - Strike the F1 key to continue. F2 to run the Setup utility.

Possible Cause — The system unit keylock is locked.

Solution — Unlock the keyboard and try again. If the problem persists, contact your service representative.

Message — Keyboard struck key failure.

Possible Cause — One or more keys are pressed or stuck.

Solution — Release the key or keys and try again. If the key is still stuck, there may be debris in the keyboard. Try to shake it loose. If the problem persists, contact your service representative.

Note: The following seven messages have the same possible cause and solution.

Message — Memory address line failure at hex-value, read hex-value, expecting hex-value.

Message — Memory data line failure at hex-value, read hex-value, expecting hex-value.

Message	Memory high address line failure at hex-value, read hex-value, expecting hex-value.
Message	Memory double word logic failure at hex-value, read hex-value, expecting hex-value.
Message	Memory odd/even logic failure at hex-value, read hex-value, expecting hex-value.
Message	Memory parity failure at hex-value, read hex-value expecting, hex-value.
Message	Memory write/read failure at hex-value, read hex-value, expecting hex-value.
Possible Cause	One of the SIMMs or associated circuitry has failed.
Solution	Check that all SIMMs are installed correctly.
Message	No boot device available – strike F1 to retry boot, F2 for the Setup utility.
Possible Cause	If booting from a floppy disk, it is nonbootable or defective, or the floppy disk drive is defective. If booting from a fixed disk, it may not be formatted as a system disk or is defective. The problem could also be in the drive controller board.
Solution	Make sure that the floppy disk in drive A or the fixed disk contains an operating system. Check the connections at both ends of the fixed disk control and data cables and reseat the drive controller. If the problem persists, contact your service representative.
Message	No boot sector on hard disk – strike F1 to retry boot, F2 for the Setup utility.
Possible Cause	The fixed disk does not contain an operating system.
Solution	Format the disk with the /S option-Caution: this procedure will destroy data on the disk. Refer to your MS-DOS Operations Reference Manual for instructions.
Message	No timer tick interrupt.
Possible Cause	The timer chip on the system board may have failed.
Solution	Contact your service representative.
Message	Not a boot diskette – strike F1 to retry boot, F2 for the Setup utility.
Possible Cause	The floppy disk in drive A is not formatted as a system floppy disk.

Solution	Replace the floppy disk with a bootable system floppy disk and try again.
Message	Shadow of System BIOS failed – Executing from ROM – Strike the F1 key to continue, F2 to run the Setup utility.
Possible Cause	The system RAM is difective.
Solution	Check the installation of the SIMMs.
Message	Shadow of Video BIOS failed – Executing from ROM – Strike the F1 key to continue, F2 to run the Setup utility.
Possible Cause	The system RAM is defective or the video BIOS cannot be shadowed.
Solution	Check the installation of all RIMMs. Rerun the Setup program and turn video BIOS shadow off.
Message	Shutdown failure.
Possible Cause	The keyboard controller or its associated logic has failed.
Solution	Contact your service representative.
Message	Time-of-day clock stopped.
Possible Cause	The intergral battery in the RTC is probably dead.
Solution	Contact your service representative.
Message	Time-of-day not set – Please run the Setup utility.
Possible Cause	The date and time information is not set in the real-time clock.
Solution	Run the Setup utility and set the date and time.
Message	Timer chip counter 2 failed.
Possible Cause	The timer chip on the system board may have failed.
Solution	Contact your service representative.
Message	Timer or interrupt controller bad.
Possible Cause	The PIT or the PICs on the system board may have failed.
Solution	Contact your service representative.

Message Unexpected interrupt in protected mode.

Possible Cause The system received an interrupt when in protected mode, probably while resting memory.

Solution Contact your service representative.

B.2.2 Post and Boot Information Messages

These messages do not indicate error conditions.

Message Hex-value Base Memory.

Meaning Indicates the amount of base memory that has been tested successfully.

Message Hex-value extended.

Meaning Indicates the amount of extended memory that has been tested successfully.

Message Decreasing available memory.

Meaning This message immediately follows any memory error message, informating you that memory modules are failing. Check that all SIMMs are installed correctly. Check expansion board memory (if installed), and check the SIMM jumpers on the system board.

Message Memory test terminated by keystroke.

Meaning The spacebar was pressed during the memory test. Reboot the system if you want to rerun the self-test.

Message Strike the F1 key to continue, F2 to run the Setup utility.

Meaning The self-test detected an error prior to boot. Pressing the F1 key lets the computer try to boot. Pressing F2 runs the Setup utility.

B.3 RUN-TIME MESSAGES

Run-time messages are displayed if an error occurs after the boot process is complete.

Message	I/O card parity interrupt at address hex-value. Type (S) hut off NMI, (R) eboot, other keys to continue.
Possible Cause	A peripheral board has failed.
Solution	Type S to shut off the nonmaskable interrupt (NMI). This will temporarily allow you to continue. If the problem persists, contact your service representative.
Message	Memory parity interrupt at address hex-value. Type (S) hut off NMI, (R) eboot, other keys to continue.
Possible Cause	One or more memory modules has failed.
Solution	Type S to shut off the nonmaskable interrupt (NMI). This will temporarily allow you to continue. Check the installation of all SIMMs. If the problem persists, contact your service representative.
Message	Unexpected HW interrupt at address hex-value. Type (R) eboot, other keys to continue.
Possible Cause	This could be any hardware-related problem.
Solution	Recheck all cables, connections, jumpers, and boards. If the problem persists, contact your service representative.
Message	Unexpected SW interrupt at addres hex-value. Type (R) eboot, other keys to continue.
Possible Cause	There is an error in the software utility.
Solution	Try turning the system off and then on again. If the problem persists, contact your software manufacturer representative.

B.4 SYSTEM BOARD ERRORS

If the POST finds an error and cannot display a message on the video display, the POST issues a series of beeps indicating the error and places a value in I/O port 80H.

For example, a failure of bit 3 in the first 64K of RAM is indicated by a 2-1-4 beep code (a burst of two beeps, a single beep, and a burst of four beeps). In addition, the POST writes a value to I/O port 80H to enable debugging tools to identify the area of failure.

Table B-1 and B-2 list the beep codes and I/O the values that the POST writes to I/O port 80H when it encounters error conditions. Table B-1 lists fatal errors (errors that halt the system). Table B-2 lists the non-fatal errors (errors that are not serious enough to half the system). Both tables list other conditions that have no beep codes.

One beep code is not listed in Table B-1 or B-2: a long beep followed by one or more short beeps indicates a video adapter filure. No beep code is sounded if a test is aborted while in progress.

Table B-1. Beep Codes for Fatal Errors

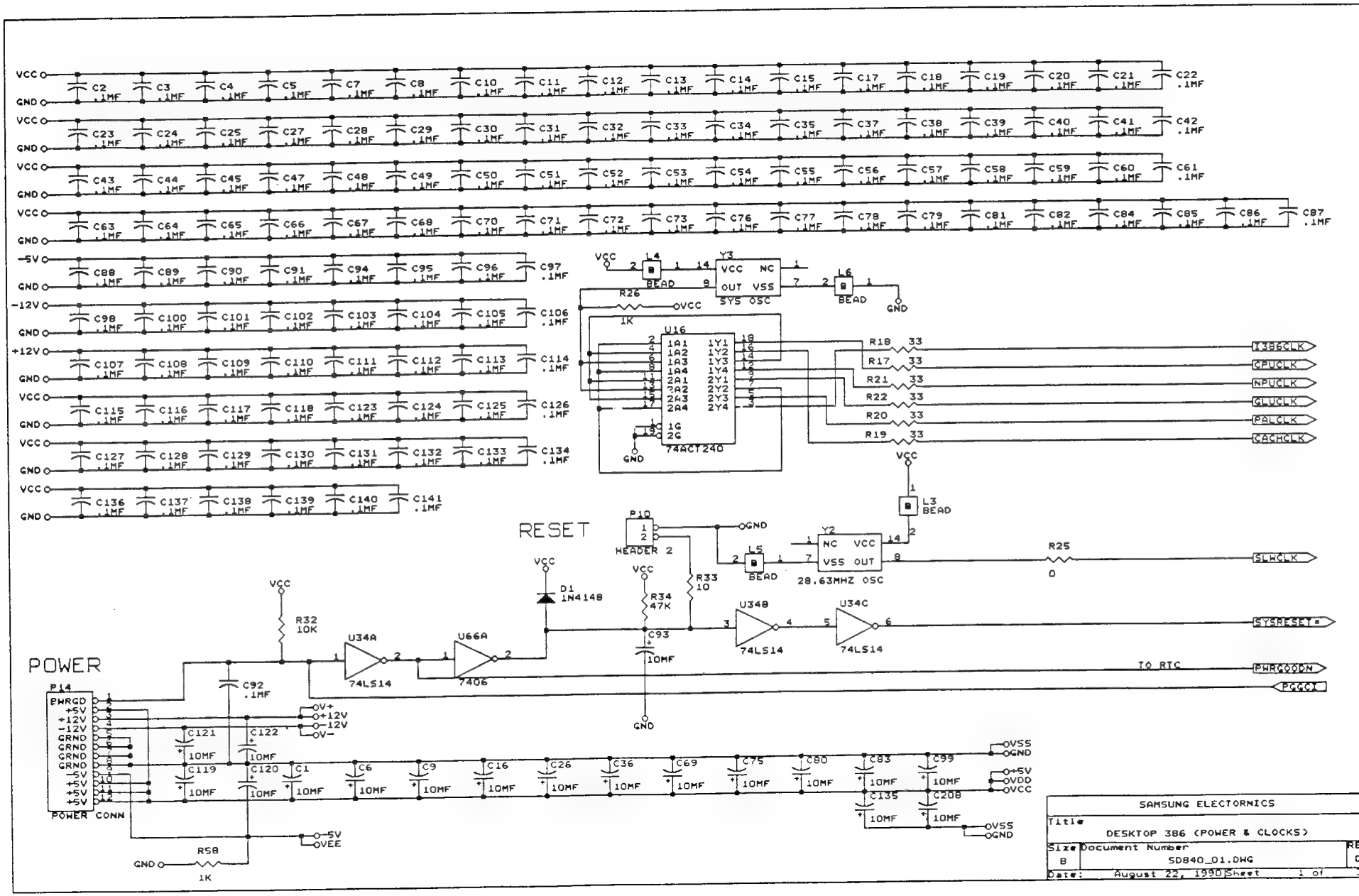
Beep Code	Description of Error	Contents of I/O Port 80H
none	386 register test in progress	01H
1-1-3	Real-time clock write/read failure	02H
1-1-4	ROM BIOS checksum failure	03H
1-2-1	Programmable Interval Timer failure	04H
1-2-2	DMA initialization failure	05H
1-2-3	DMA page register write/read failure	06H
1-3-1	RAM refresh verification failure	08H
none	1st 64K RAM test in progress	09H
1-3-3	1st 64K RAM chip or data line failure multi-bit	0AH
1-3-4	1st 64K RAM odd/even logic failure	0BH
1-4-1	1st 64K RAM address line failure	0CH
1-4-2	1st 64K RAM parity test in progress or failure	0DH
2-1-1	Bit 0 1st 64K RAM failure	10H
2-1-2	Bit 1 1st 64K RAM failure	11H
2-1-3	Bit 2 1st 64K RAM failure	12H
2-1-4	Bit 3 1st 64K RAM failure	13H
2-2-1	Bit 4 1st 64K RAM failure	14H
2-2-2	Bit 5 1st 64K RAM failure	15H
2-2-3	Bit 6 1st 64K RAM failure	16H
2-2-4	Bit 7 1st 64K RAM failure	17H
2-3-1	Bit 8 1st 64K RAM failure	18H
2-3-2	Bit 9 1st 64K RAM failure	19H
2-3-3	Bit A 1st 64K RAM failure	1AH
2-3-4	Bit B 1st 64K RAM failure	1BH
2-4-1	Bit C 1st 64K RAM failure	1CH
2-4-2	Bit D 1st 64K RAM failure	1DH
2-4-3	Bit E 1st 64K RAM failure	1EH
2-4-4	Bit F 1st 64K RAM failure	1FH
3-1-1	Slave DMA register failure	20H
3-1-2	Master DMA register failure	21H
3-1-3	Master interrupt mask register failure	22H
3-1-4	Slave interrupt mask register failure	23H
none	Intrrupt vector loading in progress	25H
3-2-4	Keyboard controller test failure	27H
none	Real-time clock power failure or checksum failure	28H

Table B-2. Beep Codes for Non-fatal Errors

Beep Code	Description of Error	Contents of I/O Port 80H
none	Real-time clock configuration	29H
3-3-4	Screen memory test failure	2BH
3-4-1	Screen initialization failure	2CH
3-4-2	Screen retrace test failure	2DH
none	Search for video ROM in progress	2EH
none	Screen running with video ROM	30H
none	Monochrome display operable	31H
none	Color display (40 column) operable	32H
none	Color display (80 column) operable	33H

C

SCHIMETIC



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Title: DESKTOP 386 (POWER & CLOCKS)

Size	Document Number	REV
B	SD840_01.DWG	D

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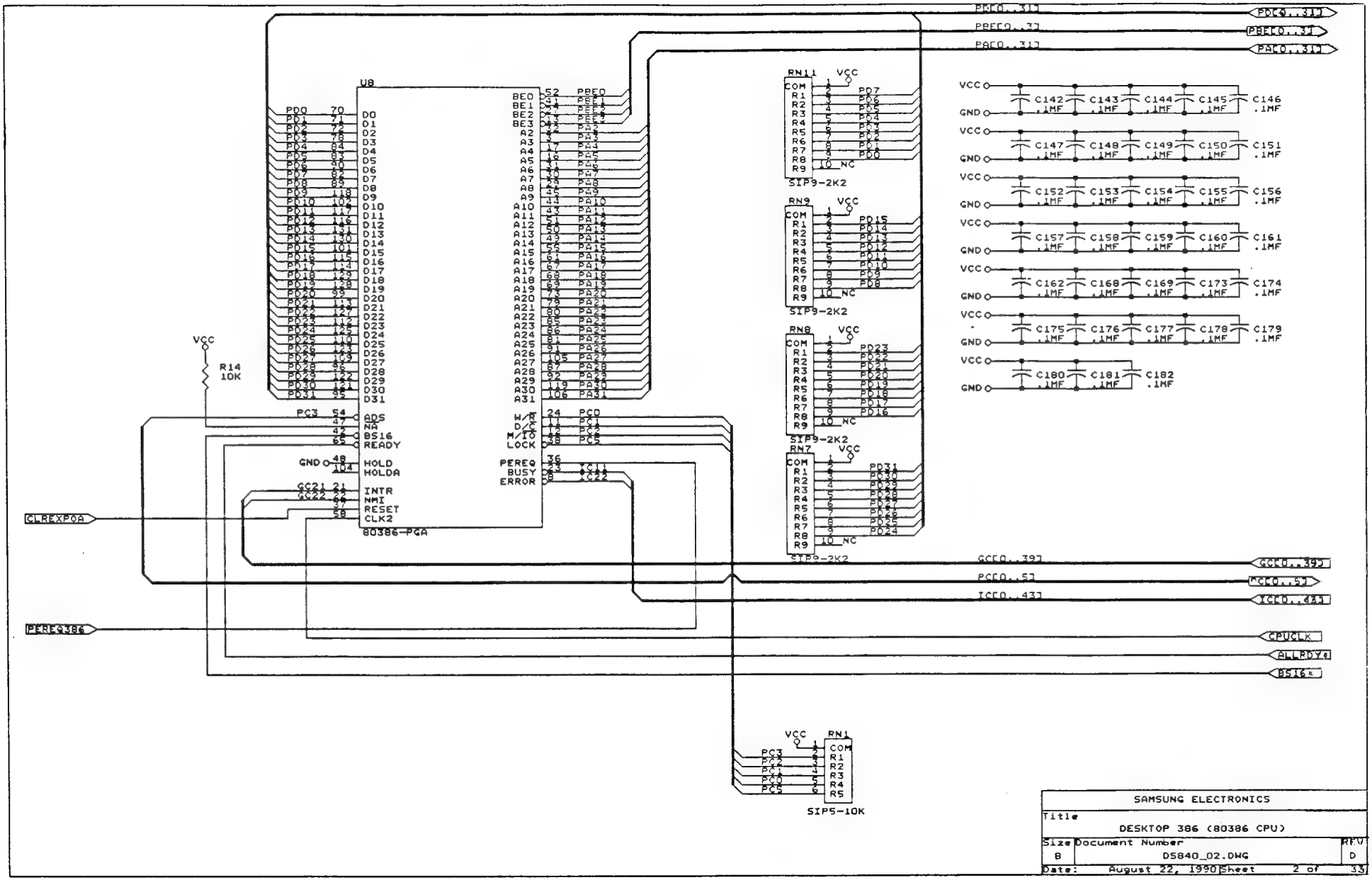
U8
80386-PGA
R14
10K
RN11
RN9
RN8
RN7
SIP9-2K2
RN1
SIP5-10K
SAMSUNG ELECTRONICS
DESKTOP 386 (80386 CPU)
D5840_02.DWG
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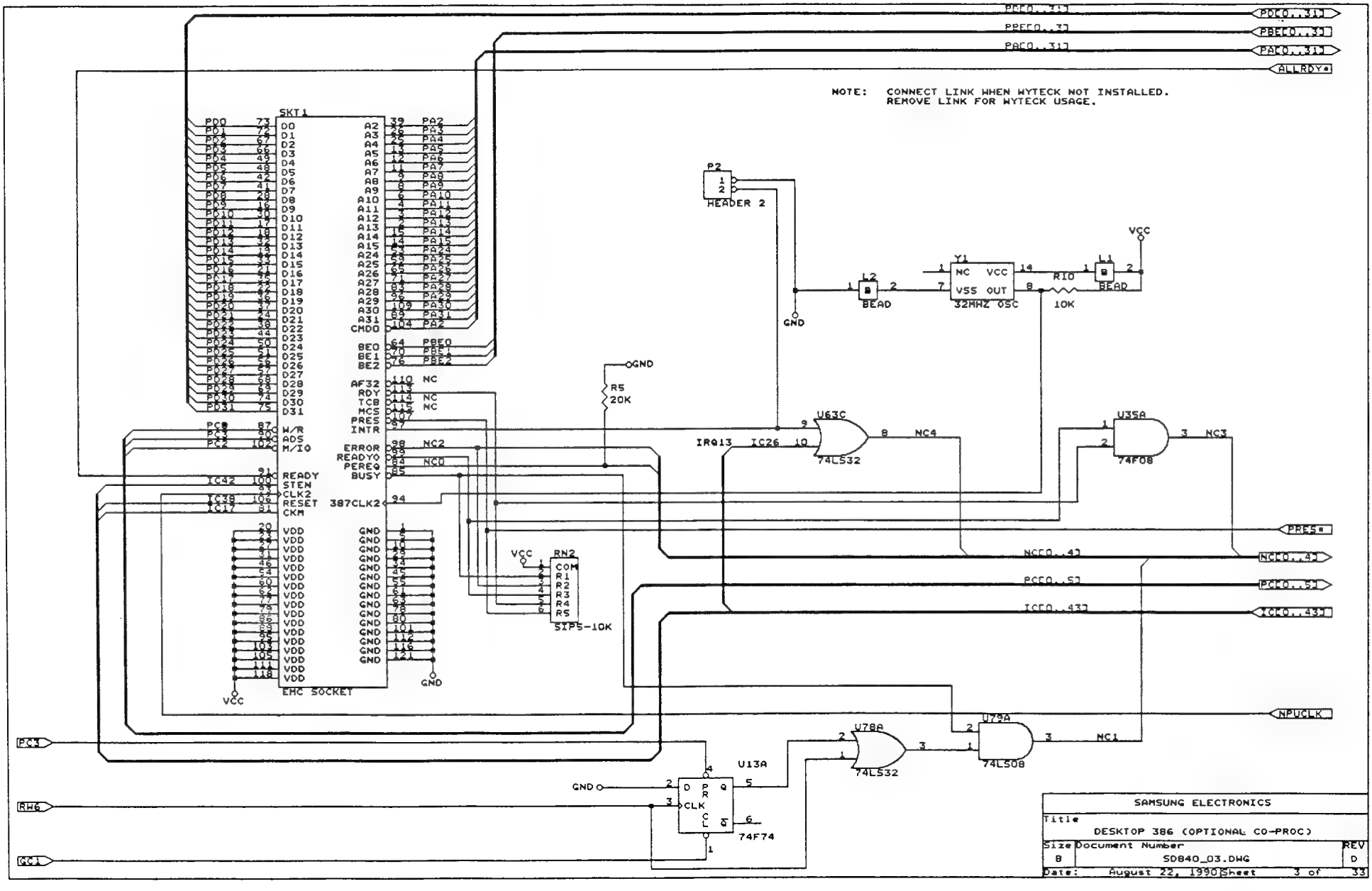
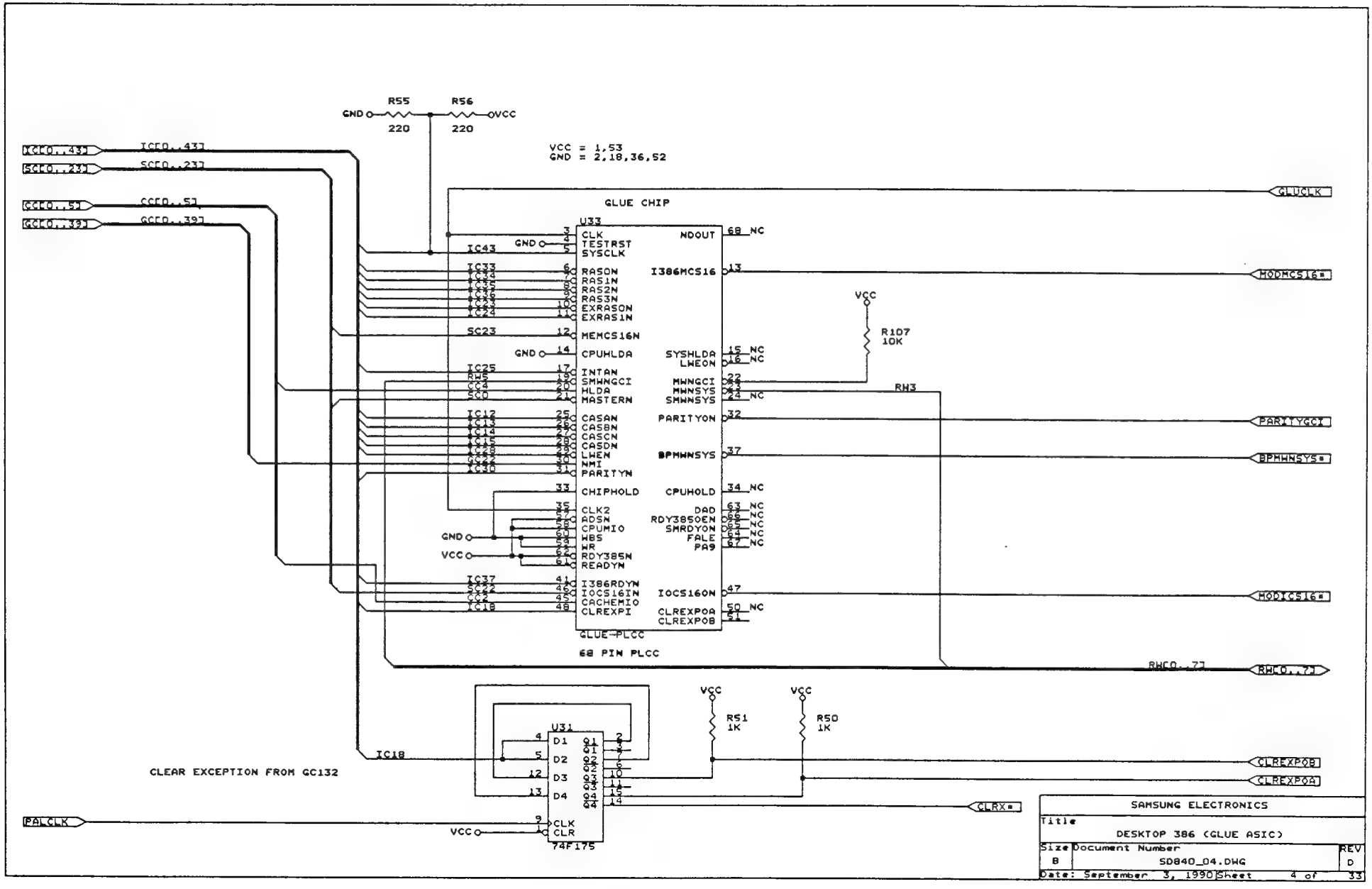
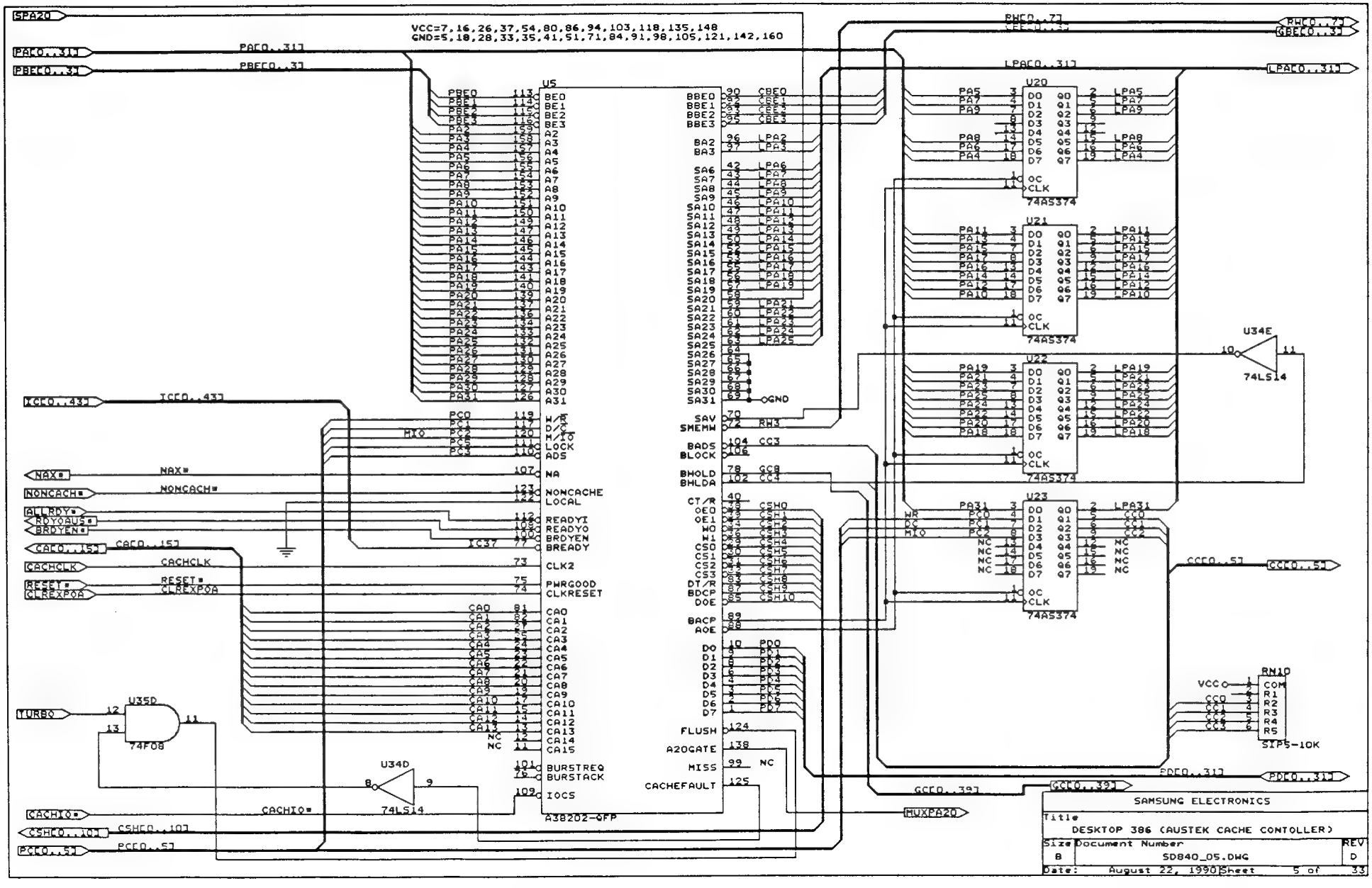


SAMSUNG ELECTRONICS		
Title: DESKTOP 386 (OPTIONAL CO-PROC)		
Size: B	Document Number: SD840_03.DWG	REV: D
Date: August 22, 1990	Sheet 3 of 33	



SAMSUNG ELECTRONICS		
Title: DESKTOP 386 (GLUE ASIC)		
Size: B	Document Number: SD840_04.DWG	REV: D
Date: September 3, 1990	Sheet 4 of 33	


SPA20
VCC=7,16,26,37,54,80,86,94,103,118,135,148
GND=5,18,28,33,35,41,51,71,84,91,98,105,121,142,160
PAC0..31
PBEC0..3
U5
A38202-GFP
U20
U21
U22
U23
74AS374
U34E
74LS14
U35D
74F08
U34D
RN10
SIP5-10K
SAMSUNG ELECTRONICS
DESKTOP 386 (AUSTEK CACHE CONTOLLER)
SD840_05.DWG
August 22, 1990
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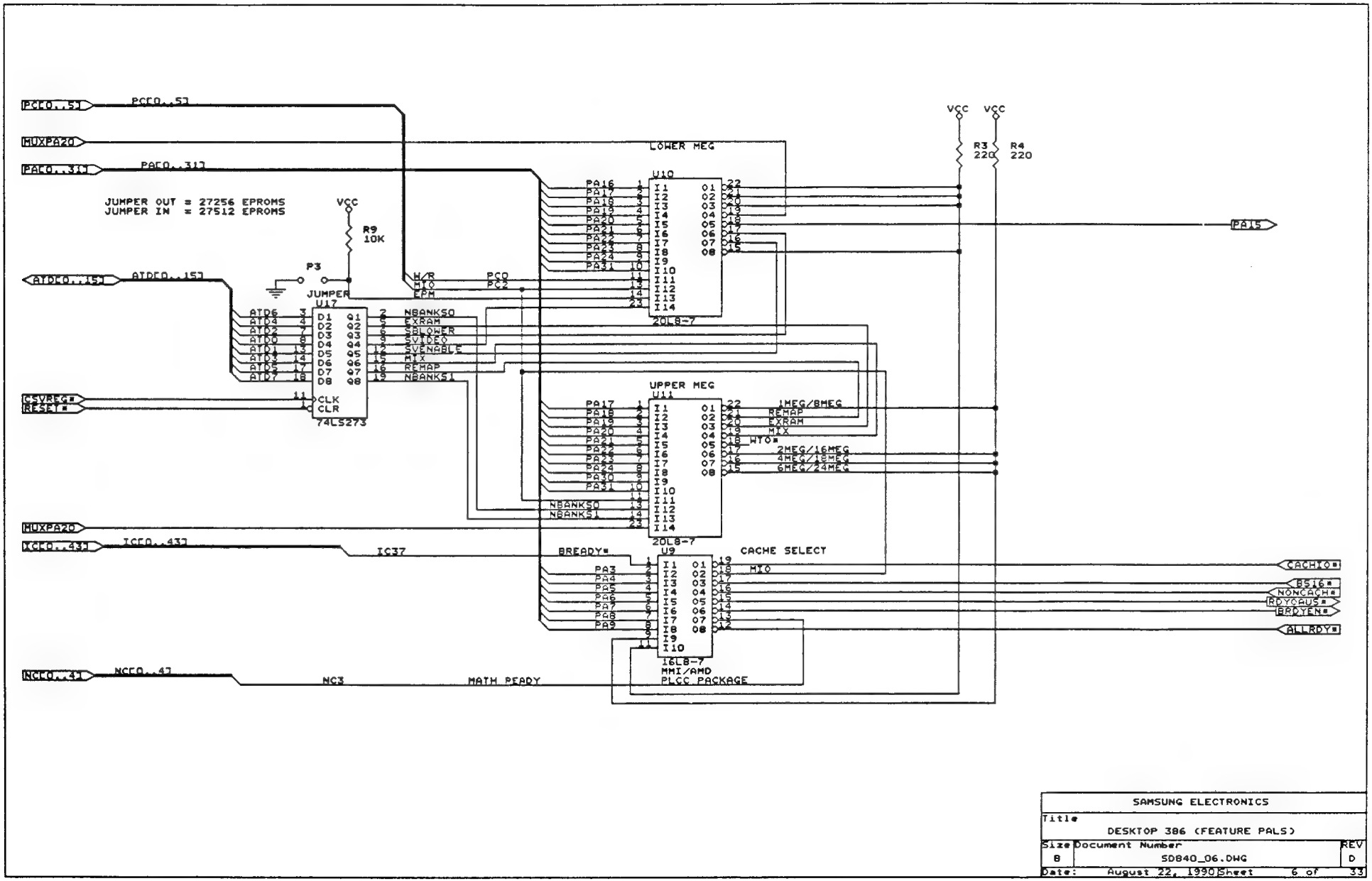
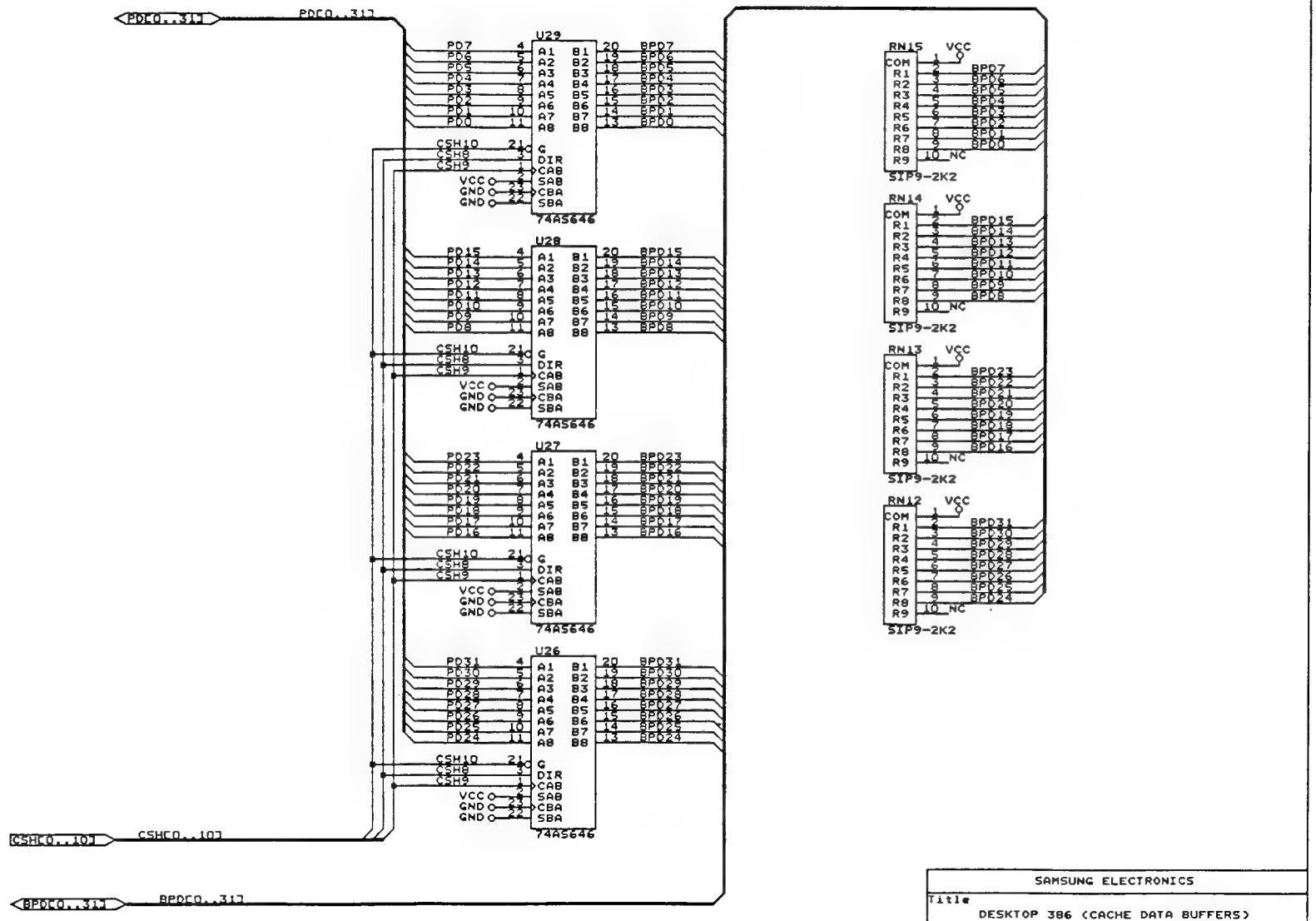
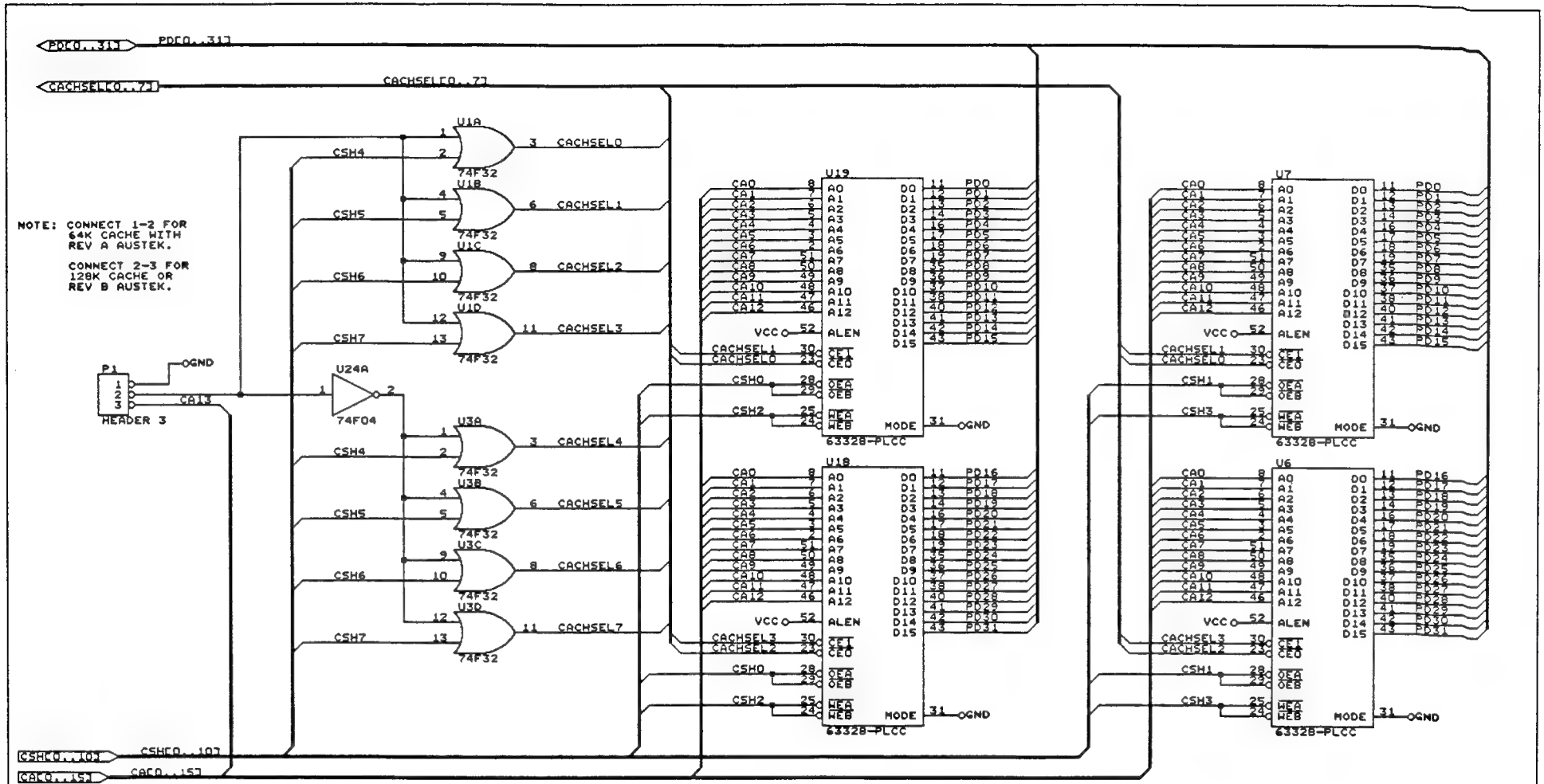


SAMSUNG ELECTRONICS		
Title: DESKTOP 386 (FEATURE PALS)		
Size: B	Document Number: SDB40_06.DWG	REV: D
Date: August 22, 1990	Sheet 6 of 33	


PDC0..31
PDC0..31
U29
PD7 4
PD6 5
PD5 6
PD4 7
PD3 8
PD2 9
PD1 10
PD0 11
A1 B1 20 BPD7
A2 B2 19 BPD6
A3 B3 18 BPD5
A4 B4 17 BPD4
A5 B5 16 BPD3
A6 B6 15 BPD2
A7 B7 14 BPD1
A8 B8 13 BPD0
CSH10 21 G
CSH8 3 DIR
CSH9 1 CAB
VCC 24 SAB
GND 23 CBA
GND 12 SBA
74AS646
U28
PD15 4
PD14 5
PD13 6
PD12 7
PD11 8
PD10 9
PD9 10
PD8 11
A1 B1 20 BPD15
A2 B2 19 BPD14
A3 B3 18 BPD13
A4 B4 17 BPD12
A5 B5 16 BPD11
A6 B6 15 BPD10
A7 B7 14 BPD9
A8 B8 13 BPD8
CSH10 21 G
CSH8 3 DIR
CSH9 1 CAB
VCC 24 SAB
GND 23 CBA
GND 12 SBA
74AS646
U27
PD23 4
PD22 5
PD21 6
PD20 7
PD19 8
PD18 9
PD17 10
PD16 11
A1 B1 20 BPD23
A2 B2 19 BPD22
A3 B3 18 BPD21
A4 B4 17 BPD20
A5 B5 16 BPD19
A6 B6 15 BPD18
A7 B7 14 BPD17
A8 B8 13 BPD16
CSH10 21 G
CSH8 3 DIR
CSH9 1 CAB
VCC 24 SAB
GND 23 CBA
GND 12 SBA
74AS646
U26
PD31 4
PD30 5
PD29 6
PD28 7
PD27 8
PD26 9
PD25 10
PD24 11
A1 B1 20 BPD31
A2 B2 19 BPD30
A3 B3 18 BPD29
A4 B4 17 BPD28
A5 B5 16 BPD27
A6 B6 15 BPD26
A7 B7 14 BPD25
A8 B8 13 BPD24
CSH10 21 G
CSH8 3 DIR
CSH9 1 CAB
VCC 24 SAB
GND 23 CBA
GND 12 SBA
74AS646
CSHC0..10
CSHC0..10
BPDC0..31
BPDC0..31
RN15 VCC
COM 1
R1 2 BPD7
R2 3 BPD6
R3 4 BPD5
R4 5 BPD4
R5 6 BPD3
R6 7 BPD2
R7 8 BPD1
R8 9 BPD0
R9 10 NC
SIP9-2K2
RN14 VCC
COM 1
R1 2 BPD15
R2 3 BPD14
R3 4 BPD13
R4 5 BPD12
R5 6 BPD11
R6 7 BPD10
R7 8 BPD9
R8 9 BPD8
R9 10 NC
SIP9-2K2
RN13 VCC
COM 1
R1 2 BPD23
R2 3 BPD22
R3 4 BPD21
R4 5 BPD20
R5 6 BPD19
R6 7 BPD18
R7 8 BPD17
R8 9 BPD16
R9 10 NC
SIP9-2K2
RN12 VCC
COM 1
R1 2 BPD31
R2 3 BPD30
R3 4 BPD29
R4 5 BPD28
R5 6 BPD27
R6 7 BPD26
R7 8 BPD25
R8 9 BPD24
R9 10 NC
SIP9-2K2
SAMSUNG ELECTRONICS
Title
DESKTOP 386 (CACHE DATA BUFFERS)
Size B
Document Number SD840_07.DWG
REV D
Date: August 22, 1990 Sheet 7 of 33



NOTE: THESE RAMS ARE SURFACE MOUNTED TO THE BOARD

SAMSUNG ELETRONICS		
Title: DESKTOP 386 (64K CACHE RAM)		
Size: B	Document Number: SD840_08.DWG	REV: D
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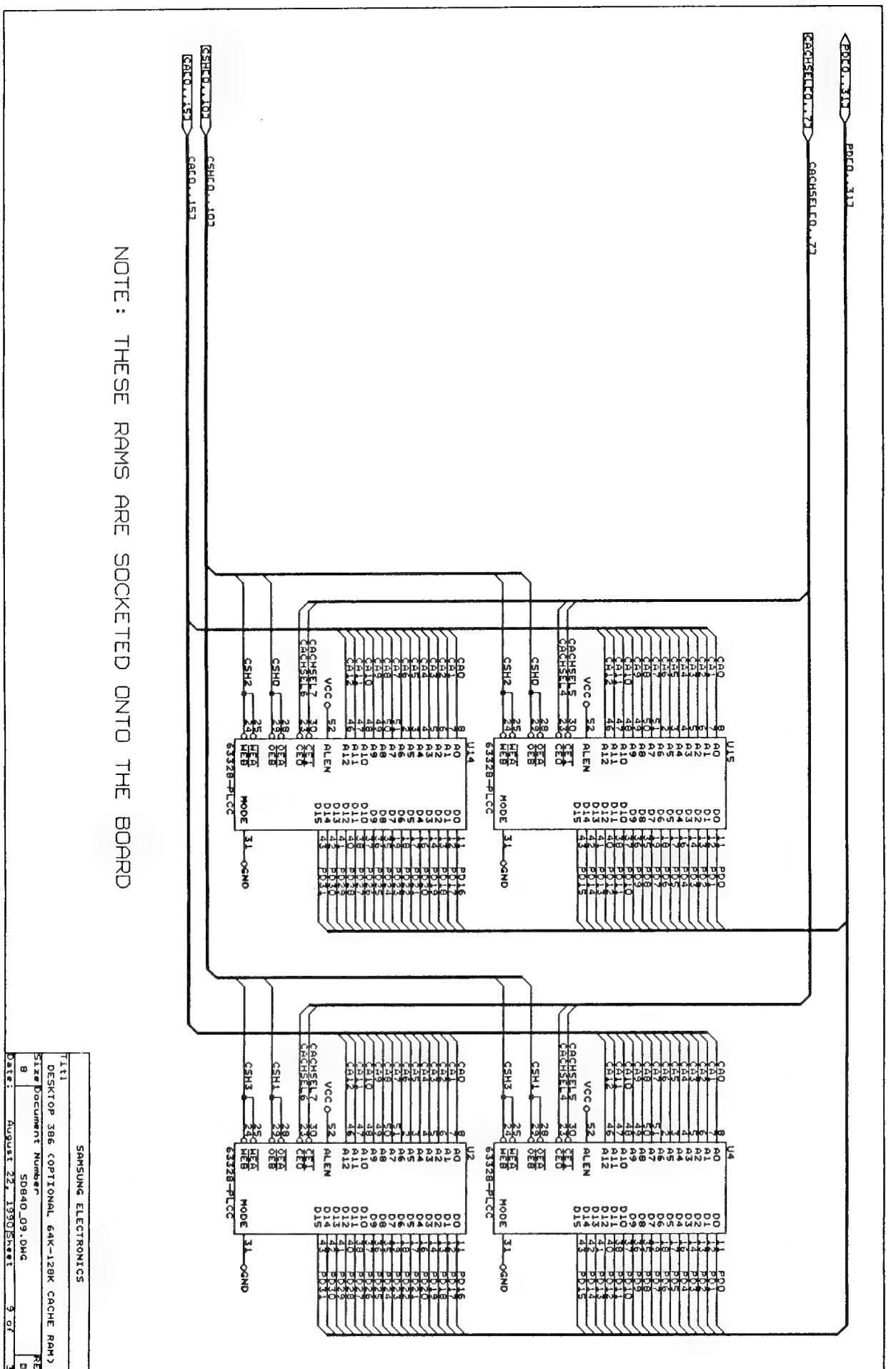
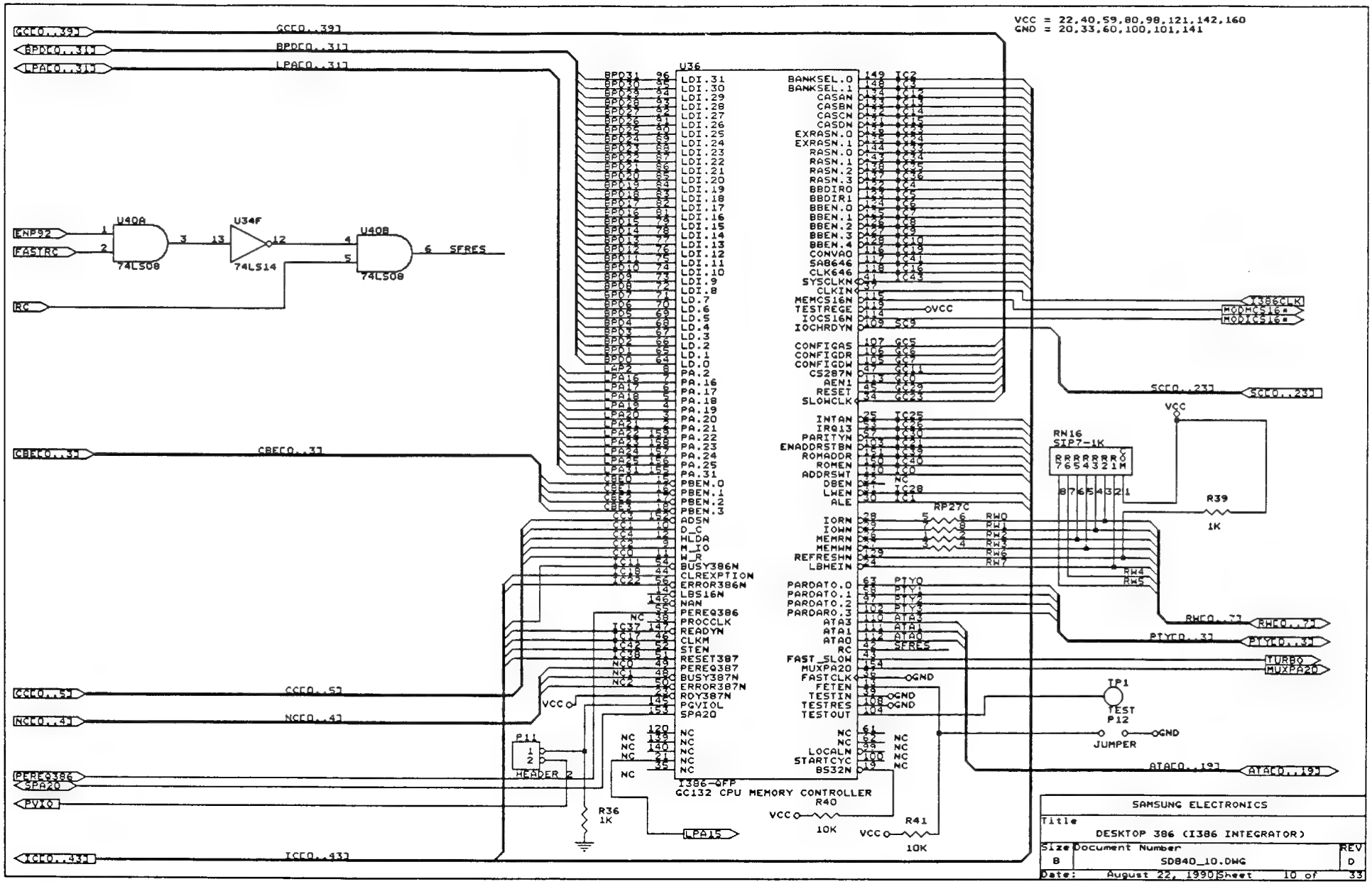
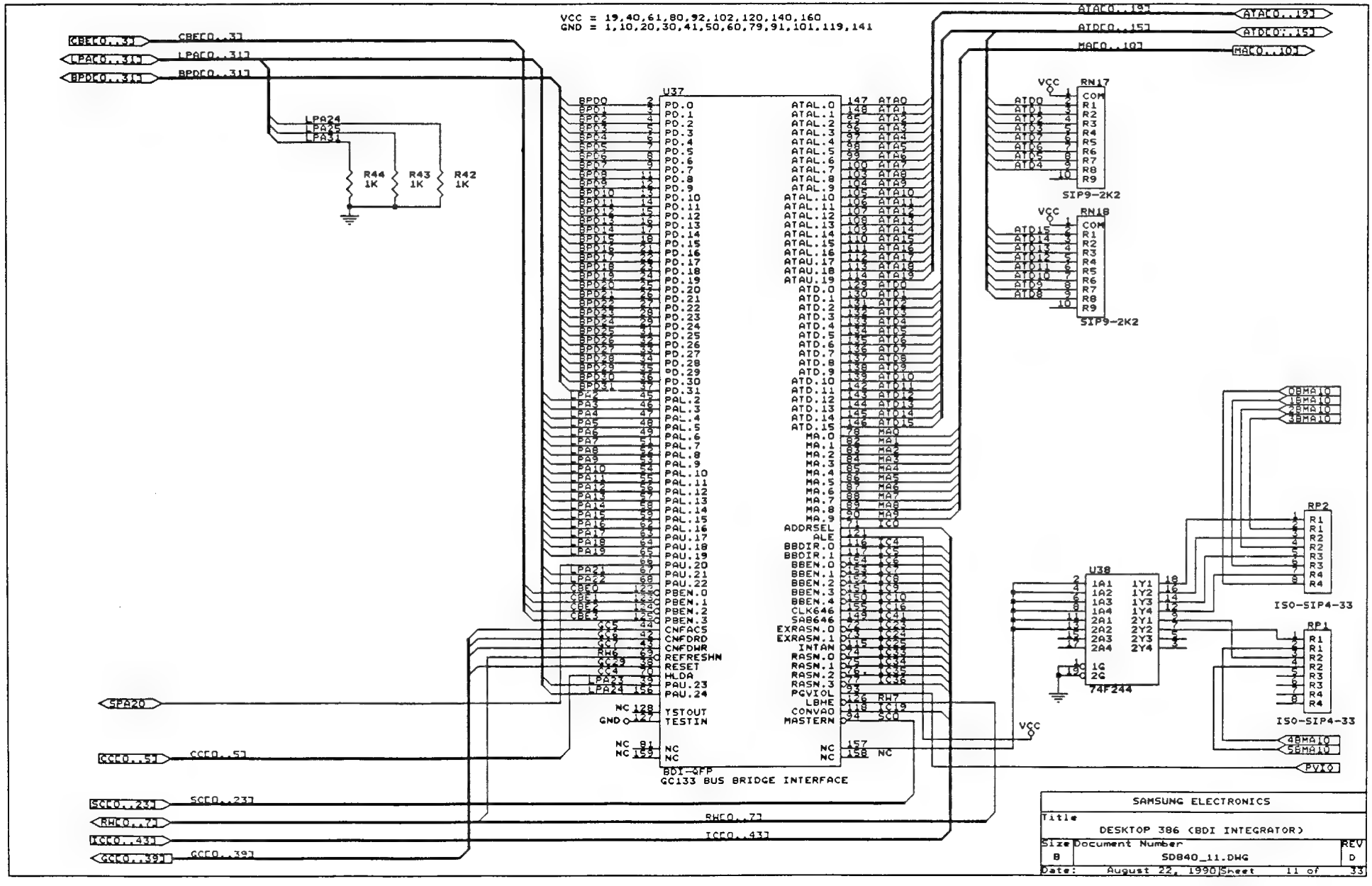

NOTE: THESE RAMS ARE SOCKETED ONTO THE BOARD
SAMSUNG ELECTRONICS
Title
DESKTOP 386 (OPTIONAL 64K-128K CACHE RAM)
Size Document Number
B
SD840_09.DWG
REV
D
Date: August 22, 1990 Sheet 9 of 33


VCC = 22,40,59,80,98,121,142,160
GND = 20,33,60,100,101,141
U36
I386-QFP
GC132 CPU MEMORY CONTROLLER
U40A
74LS08
U34F
74LS14
U40B
74LS08
ENP92
FASTRC
SFRES
RC
R36 1K
R40 10K
R41 10K
P11
HEADER 2
RP27C
RN16 SIP7-1K
R39 1K
IP1
TEST P12
JUMPER
SAMSUNG ELECTRONICS
Title
DESKTOP 386 (I386 INTEGRATOR)
Size B
Document Number SD840_10.DWG
REV D
Date: August 22, 1990 Sheet 10 of 33


VCC = 19,40,61,80,92,102,120,140,160
GND = 1,10,20,30,41,50,60,79,91,101,119,141
U37
BDI-QFP
GC133 BUS BRIDGE INTERFACE
RN17
RN18
SIP9-2K2
R44 1K
R43 1K
R42 1K
U38
74F244
RP2
RP1
ISO-SIP4-33
SPA20
SCFO..23J
RHFO..7J
ICFO..43J
GCFO..39J
CCFO..5J
PVIO
SAMSUNG ELECTRONICS
DESKTOP 386 (BDI INTEGRATOR)
SD840_11.DWG
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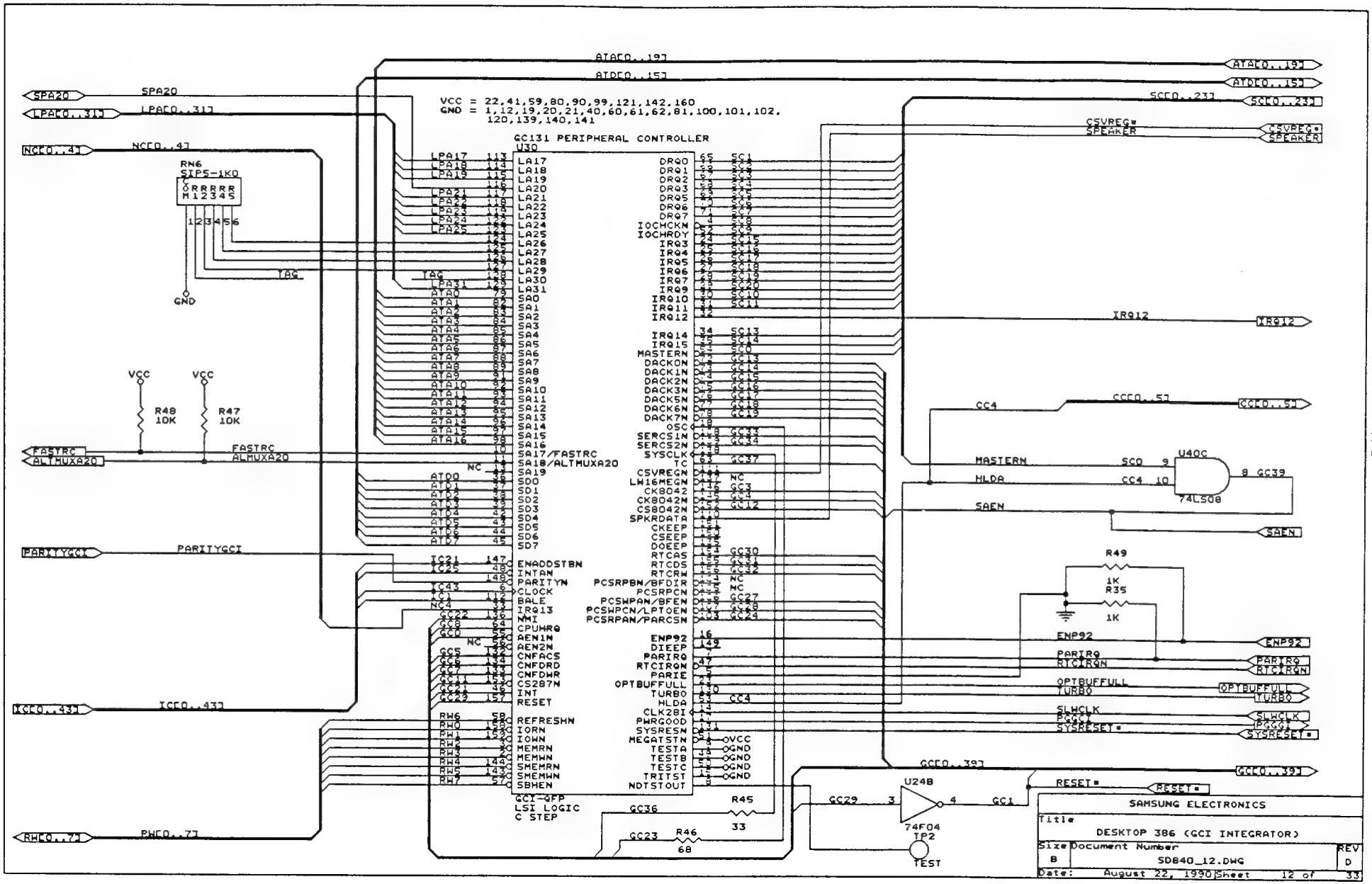
VCC = 22,41,59,80,90,99,121,142,160
GND = 1,12,19,20,21,40,60,61,62,81,100,101,102,120,139,140,141
GC131 PERIPHERAL CONTROLLER
U30
GCI-QFP
LSI LOGIC
C STEP
SAMSUNG ELECTRONICS
Title
DESKTOP 386 (GCI INTEGRATOR)
Size B
Document Number SD840_12.DWG
REV D
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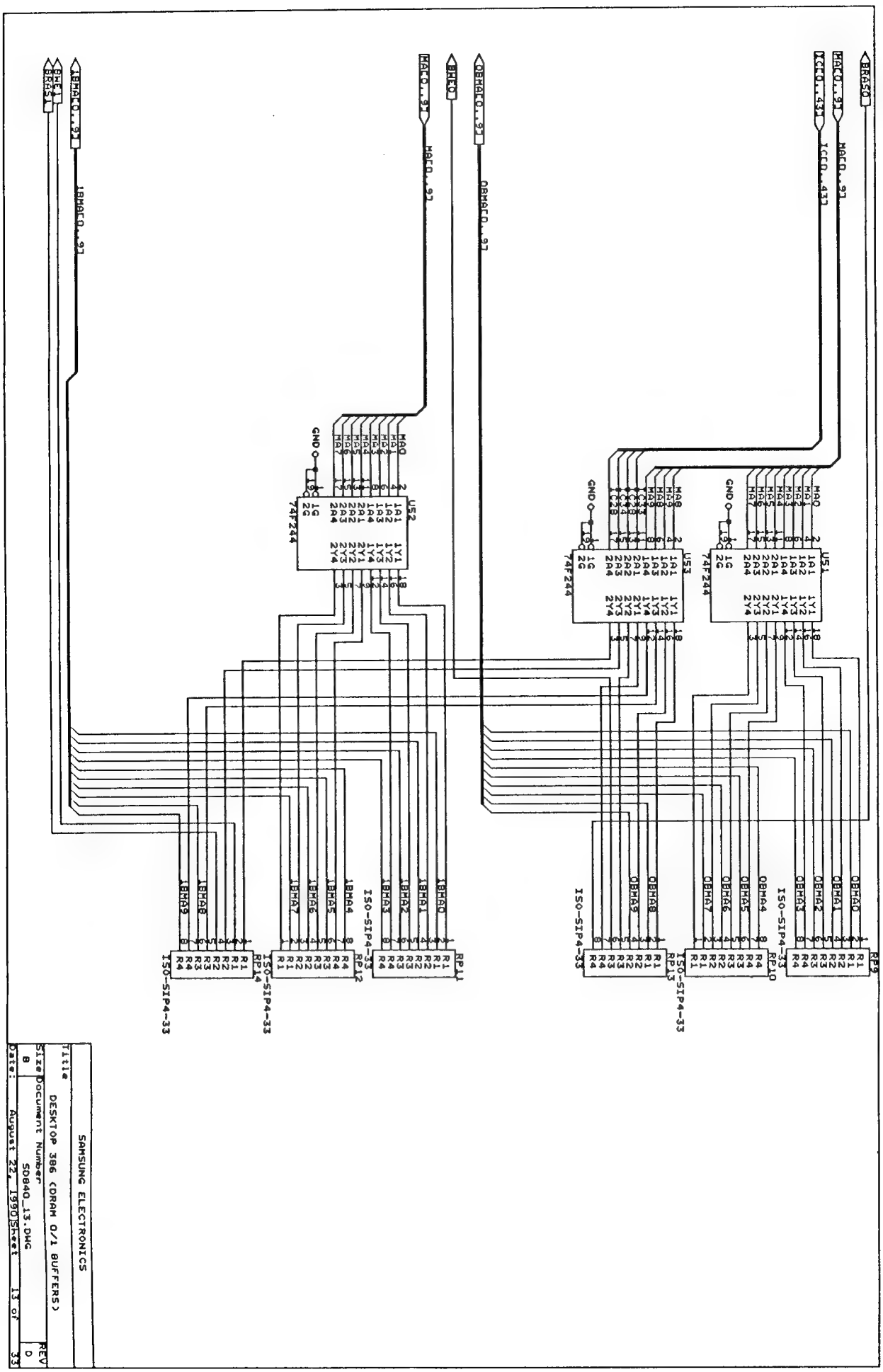
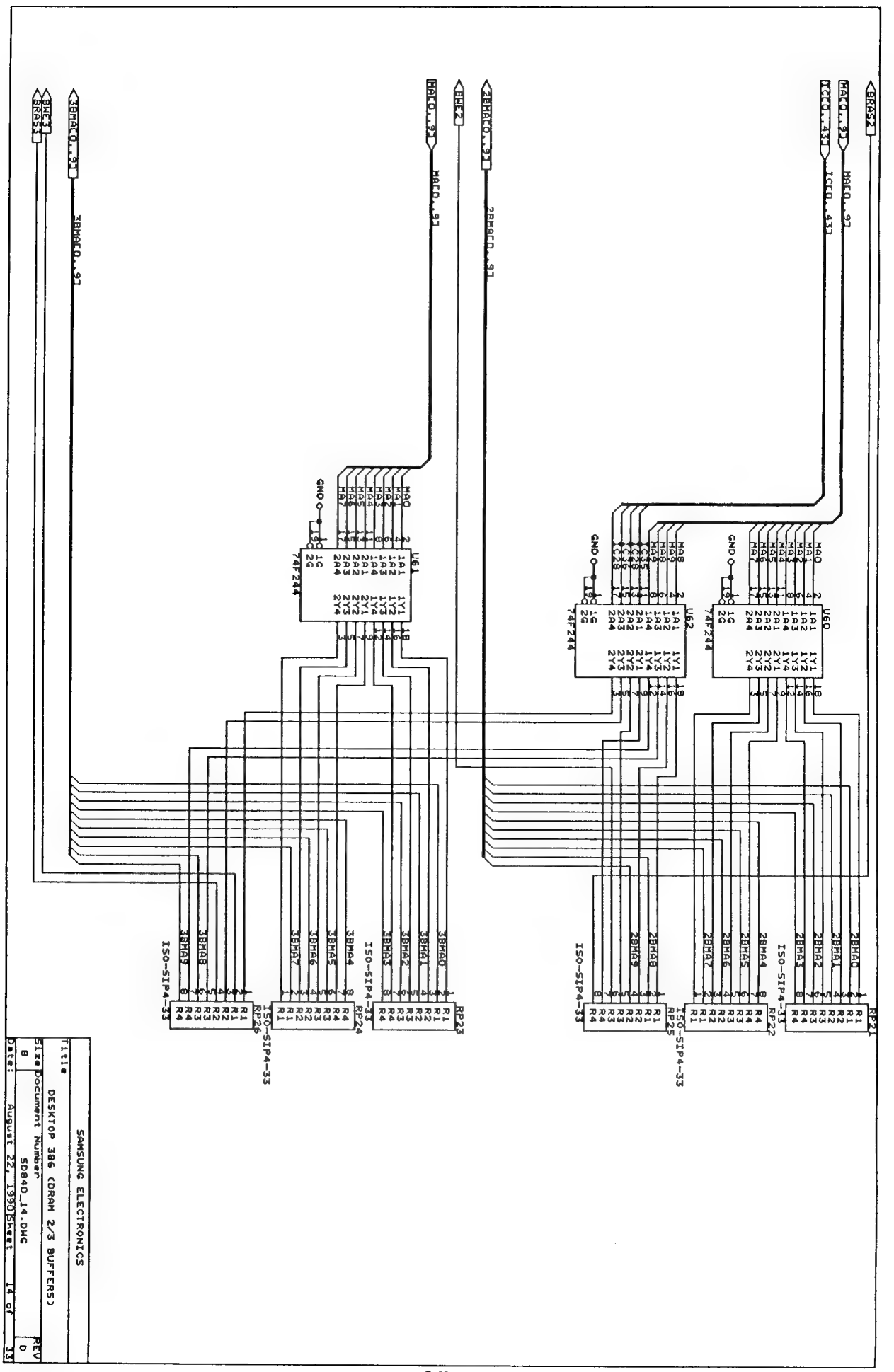

SAMSUNG ELECTRONICS
DESKTOP 386 (DRAM I/O BUFFERS)
SD840_13.DWG
August 22, 1990
74F244
ISO-SIP4-33


SAMSUNG ELECTRONICS
Title
DESKTOP 386 (DRAM 2/3 BUFFERS)
Size: B
Document Number: SD840_14.DWG
REV: D
Date: August 22, 1990
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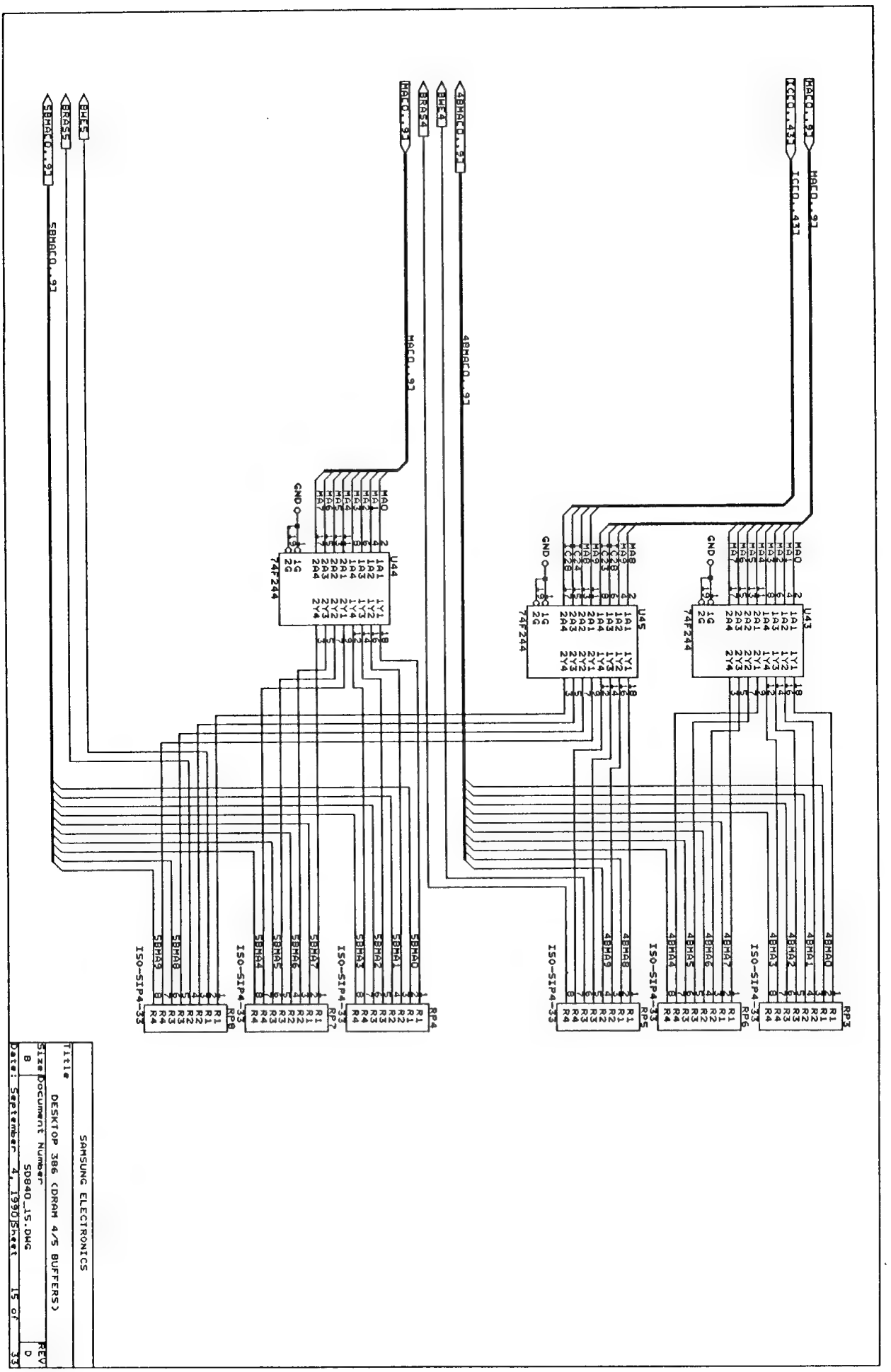
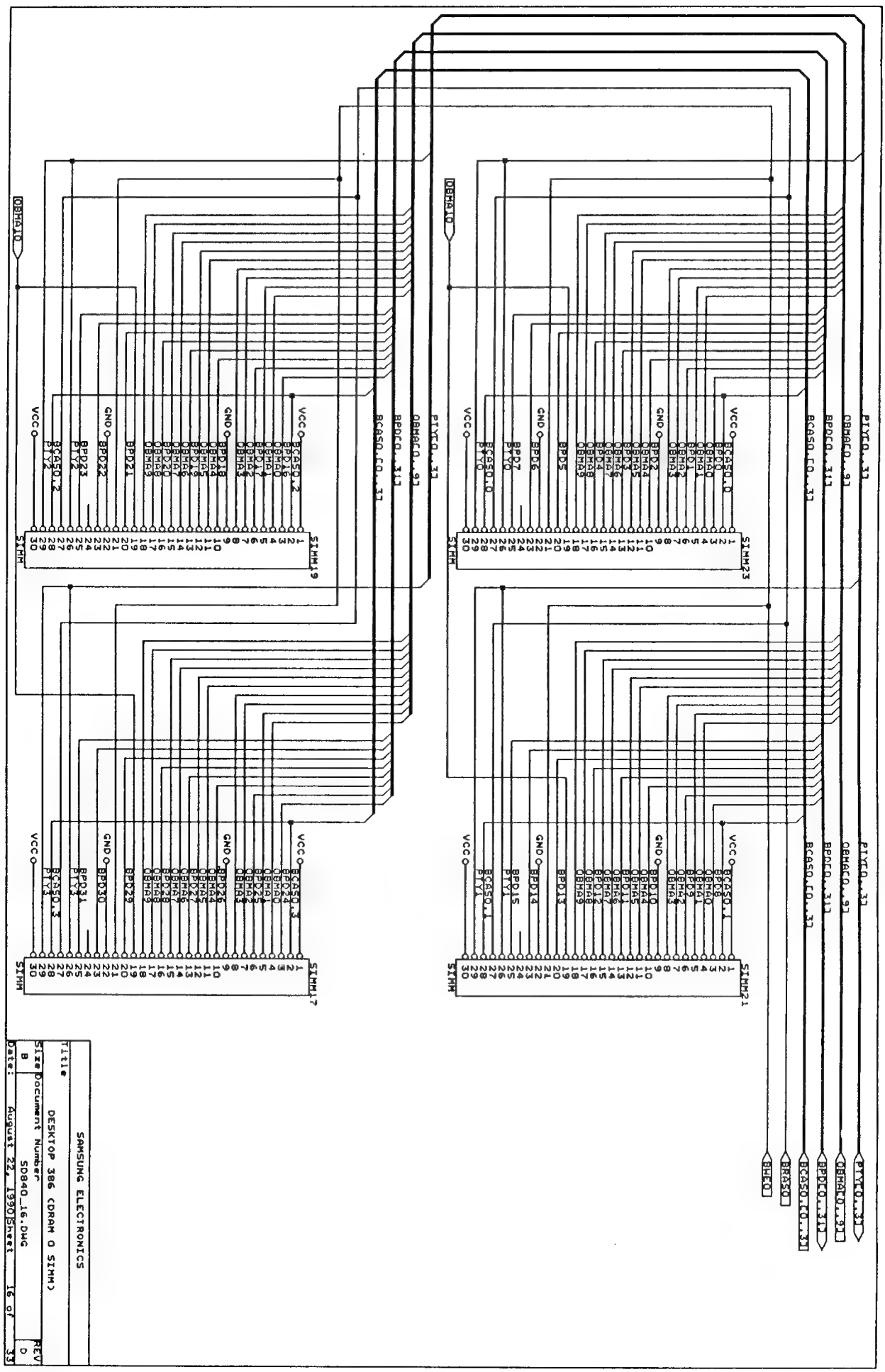
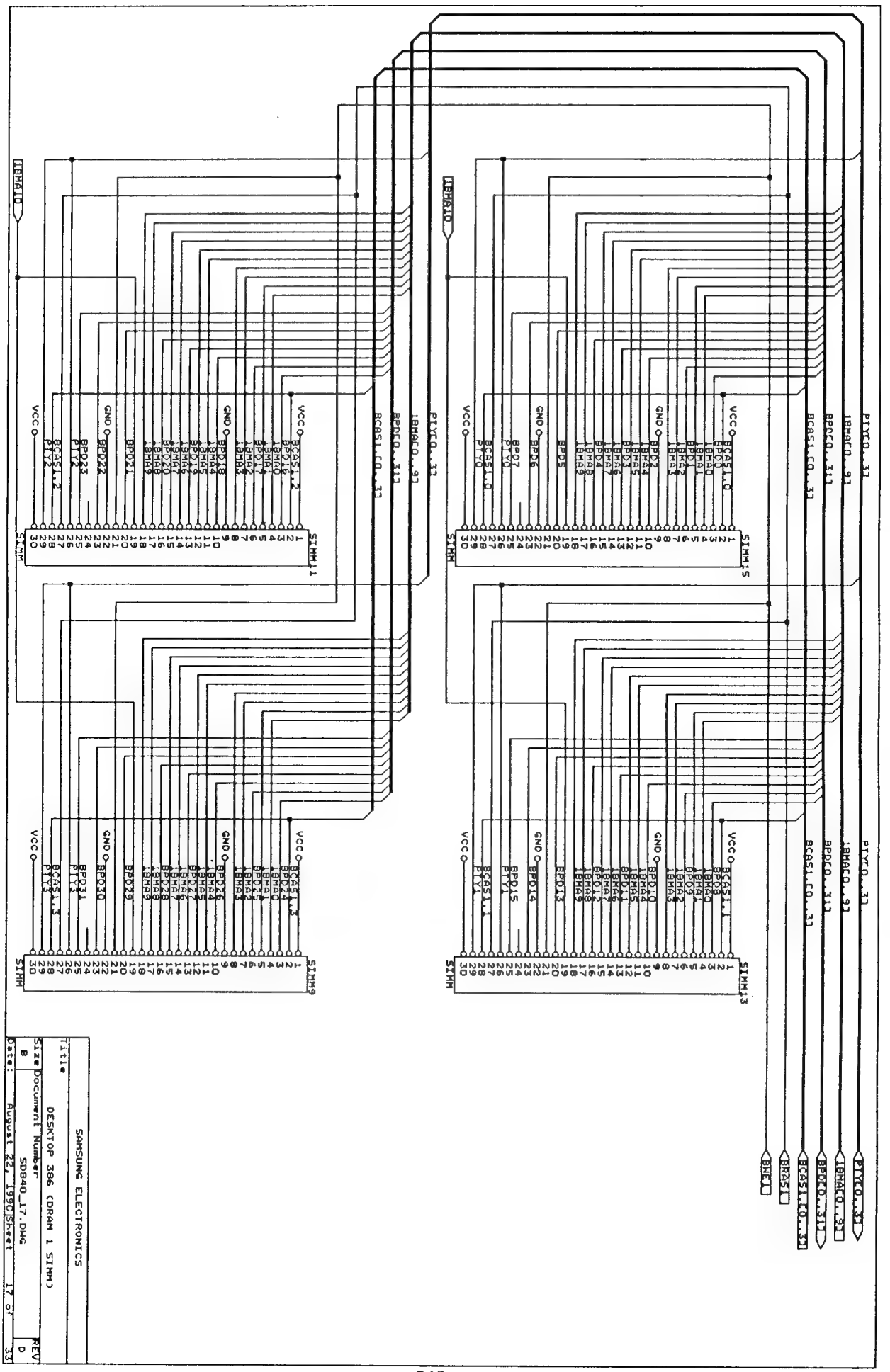

MA[0..9]
MAC[0..9]
ICC[0..43]
48MA[0..9]
48MAC[0..9]
BRAS4
BHE4
BRAS5
BHE5
GND
74F244
U43
U44
U45
ISO-SIP4-33
RP3
RP4
RP5
RP6
RP7
RP8
Title
DESKTOP 386 (DRAM 4/5 BUFFERS)
SAMSUNG ELECTRONICS
Size
B
Document Number
SD840_15.DWG
REV
D
Date: September 4, 1990
Sheet 15 of 33


SAMSUNG ELECTRONICS
Title
DESKTOP 386 CORAM 0 SIMM)
Size B
Document Number SD840_16.DWG
REV 0
Date: August 22, 1990 Sheet 16 of 33


SAMSUNG ELECTRONICS
DESKTOP 386 (DRAM 1 SIMM)
SD840_17.DWG
August 22, 1990
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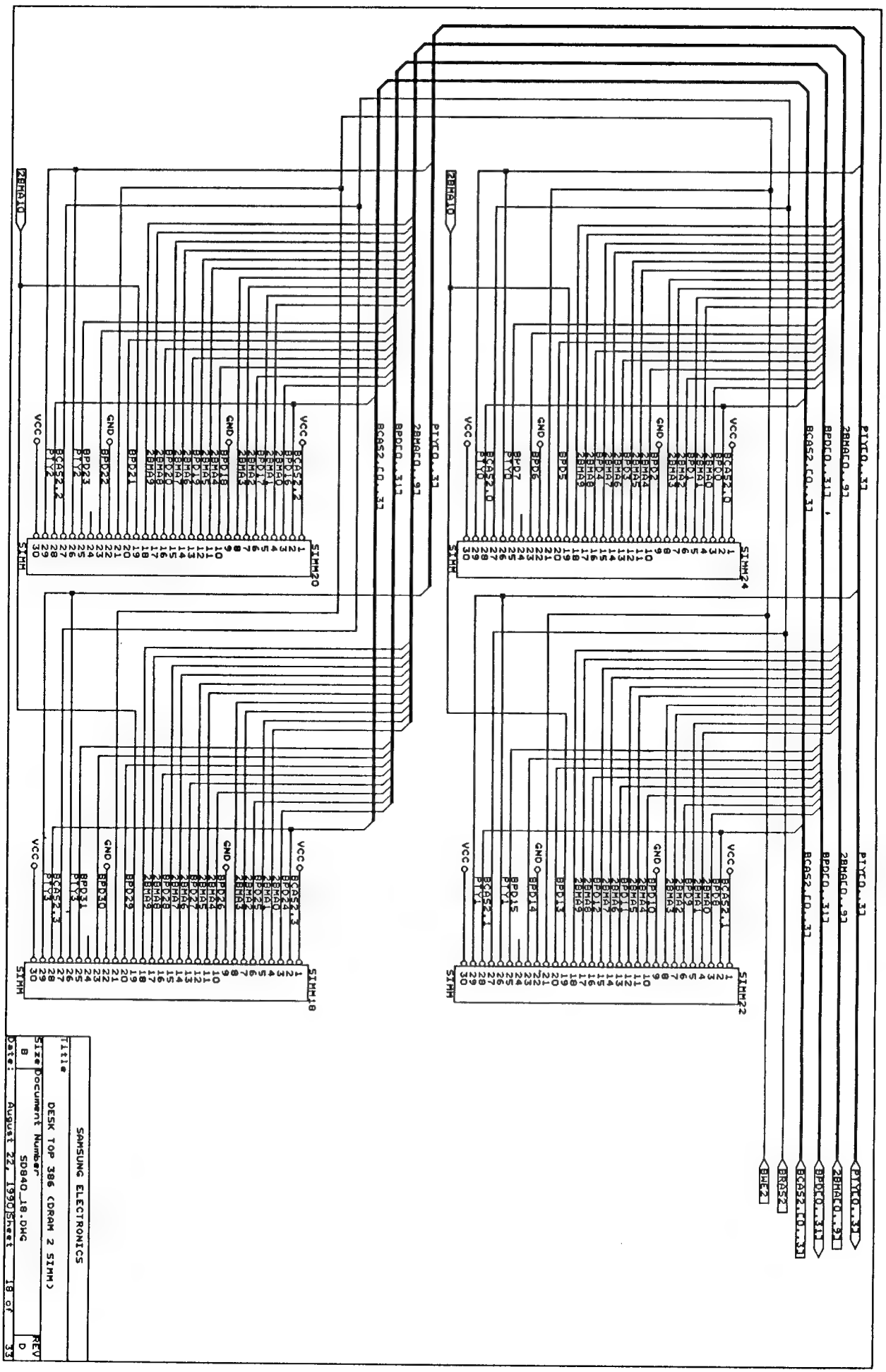
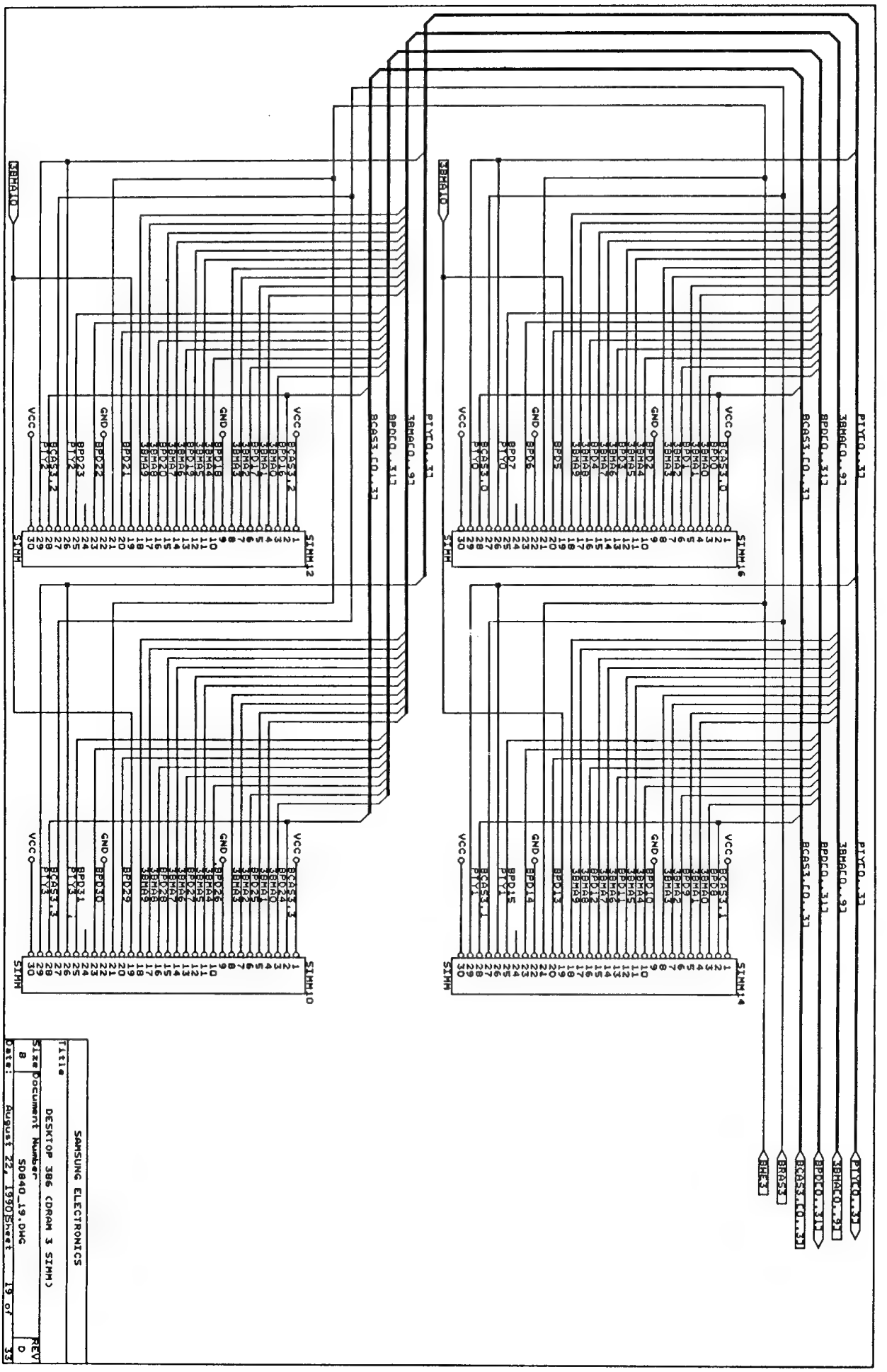
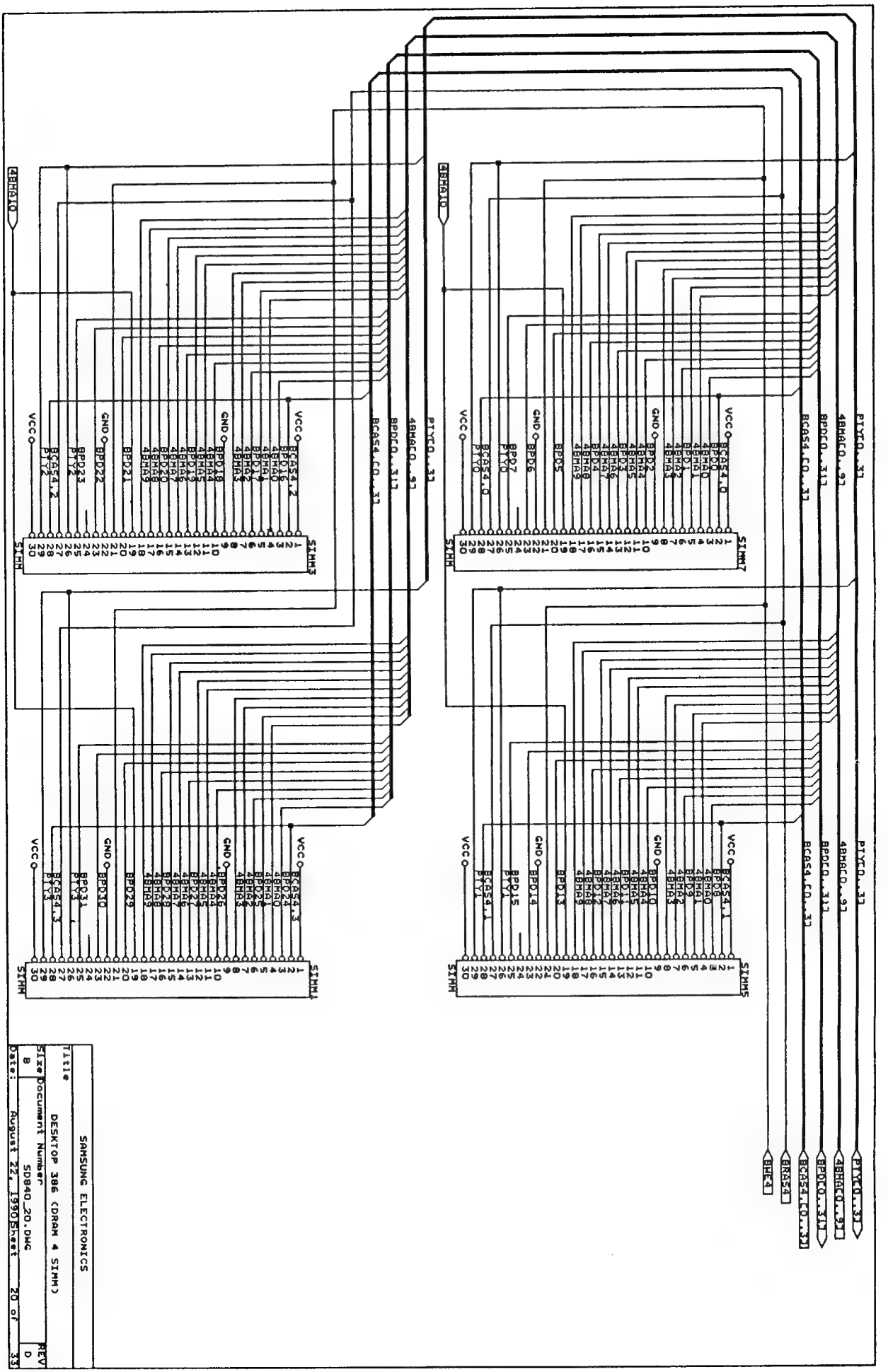

SAMSUNG ELECTRONICS
Title
DESK TOP 386 (DRAM 2 SIMM)
Size
B
Document Number
SD840_18.DWG
REV
D
Date: August 22, 1990
Sheet 18 of 33


SAMSUNG ELECTRONICS
DESKTOP 386 (DRAM 3 SIMM)
Size: B
Document Number: SD840_19.DWG
REV: D
Date: August 22, 1990
Sheet 19 of 33


SAMSUNG ELECTRONICS
Title
DESKTOP 386 (DRAM 4 SIMM)
Size
B
Document Number
50840_20.DWG
REV
D
Date:
August 22, 1990
Sheet
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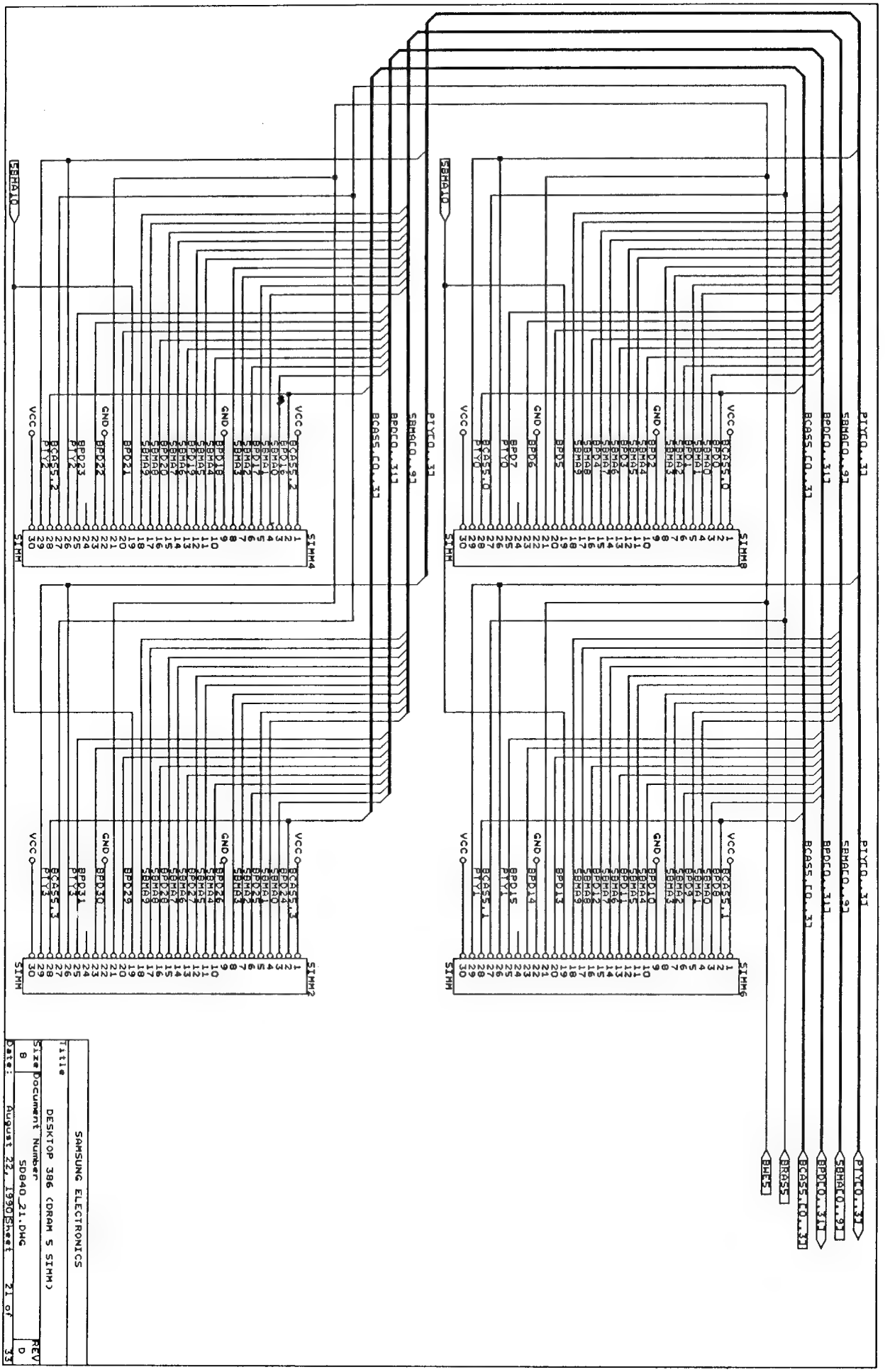
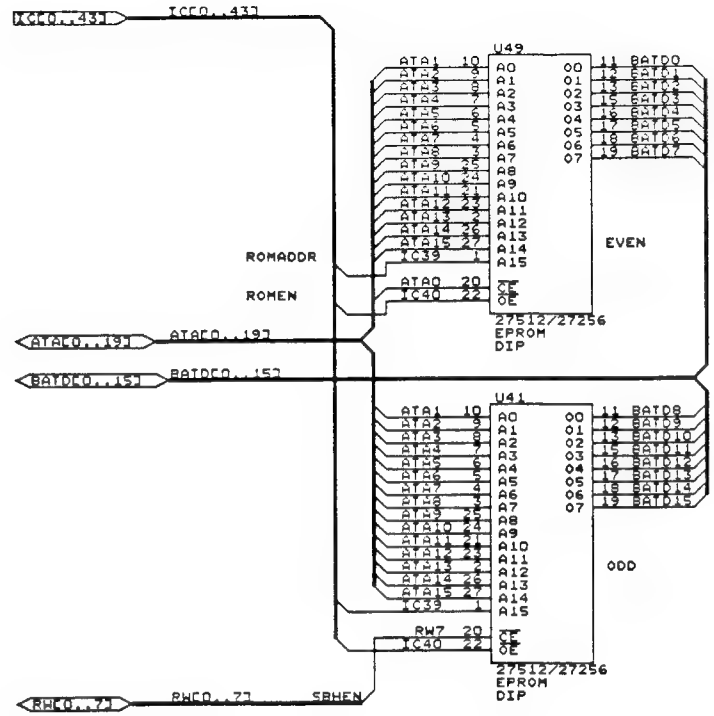
33


SAMSUNG ELECTRONICS
Title
DESKTOP 386 (DRAM 5 SIMM)
Size Document Number
B SD840_21.DMG
Date: August 22, 1990 Sheet 21 of 33
REV
D



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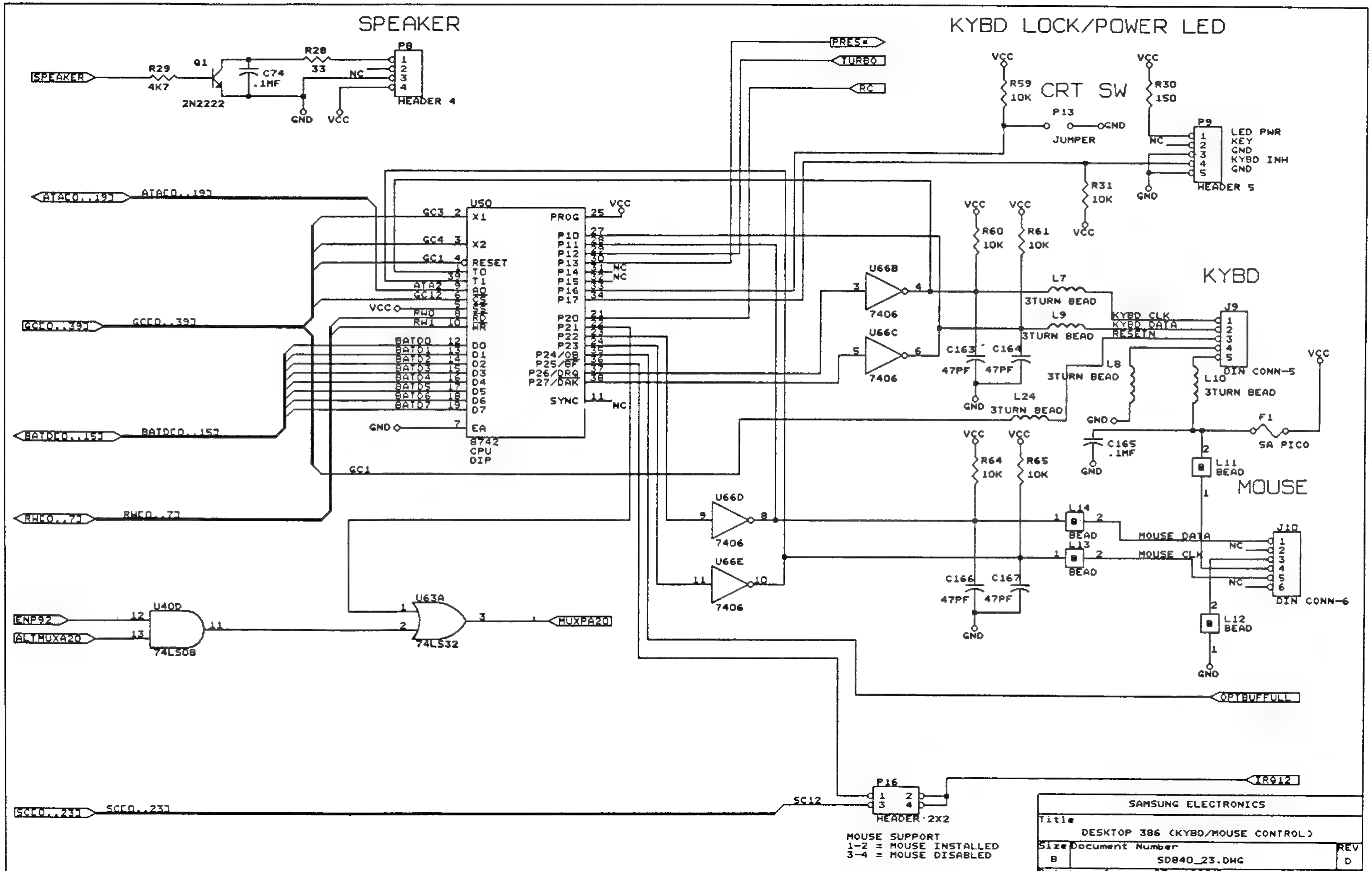
SAMSUNG ELECTRONICS		
Title: DESKTOP 386 (EPROM)		
Size: B	Document Number: SD840_22.DWG	REV: D
Date: August 22, 1990	Sheet 22 of 33	


SPEAKER
KYBD LOCK/POWER LED
CRT SW
KYBD
MOUSE
SPEAKER
R29
4K7
Q1
2N2222
C74
.1MF
R28
33
P8
HEADER 4
NC
GND
VCC
R59
10K
P13
JUMPER
R30
150
P9
LED PWR
KEY
GND
KYBD INH
GND
HEADER 5
R31
10K
ATA[0..19]
GC[0..39]
BAT[0..15]
RW[0..7]
U50
8742
CPU
DIP
X1
X2
RESET
T0
T1
A0
CS
SS
RD
WR
D0
D1
D2
D3
D4
D5
D6
D7
EA
PROG
P10
P11
P12
P13
P14
P15
P16
P17
P20
P21
P22
P23
P24/OB
P25/BF
P26/DRQ
P27/DAK
SYNC
GC3
GC4
GC1
ATA2
GC12
RW0
RW1
BATD0
BATD1
BATD2
BATD3
BATD4
BATD5
BATD6
BATD7
PRES*
TURBO
RC
U66B
U66C
U66D
U66E
7406
R60
10K
R61
10K
R64
10K
R65
10K
C163
C164
47PF
C166
C167
L7
L9
L8
L10
L24
3TURN BEAD
KYBD CLK
KYBD DATA
RESETN
J9
DIN CONN-5
C165
.1MF
F1
SA PICO
L11
L12
L13
L14
BEAD
MOUSE DATA
MOUSE CLK
J10
DIN CONN-6
U40D
74LS08
ENP92
ALTMUXA20
U63A
74LS32
MUXPA20
OPTBUFFULL
IRQ12
SC[0..23]
SC12
P16
HEADER 2X2
MOUSE SUPPORT
1-2 = MOUSE INSTALLED
3-4 = MOUSE DISABLED
SAMSUNG ELECTRONICS
Title
DESKTOP 386 (KYBD/MOUSE CONTROL)
Size B
Document Number
SD840_23.DWG
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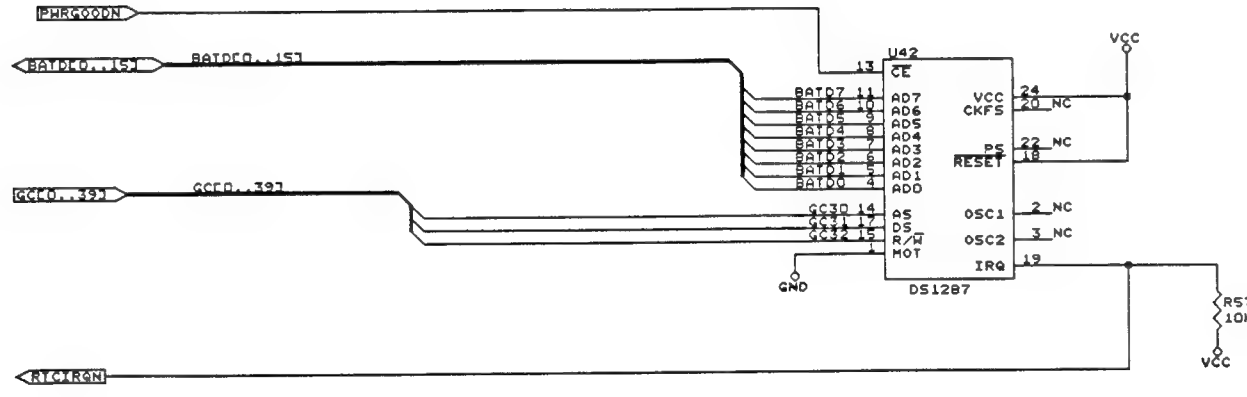
Date: August 23, 1990
Sheet 23 of 33



SAMSUNG ELECTRONICS		
Title: DESKTOP 386 (REAL TIME CLOCK)		
Size: B	Document Number: SD840_24.DWG	REV: D
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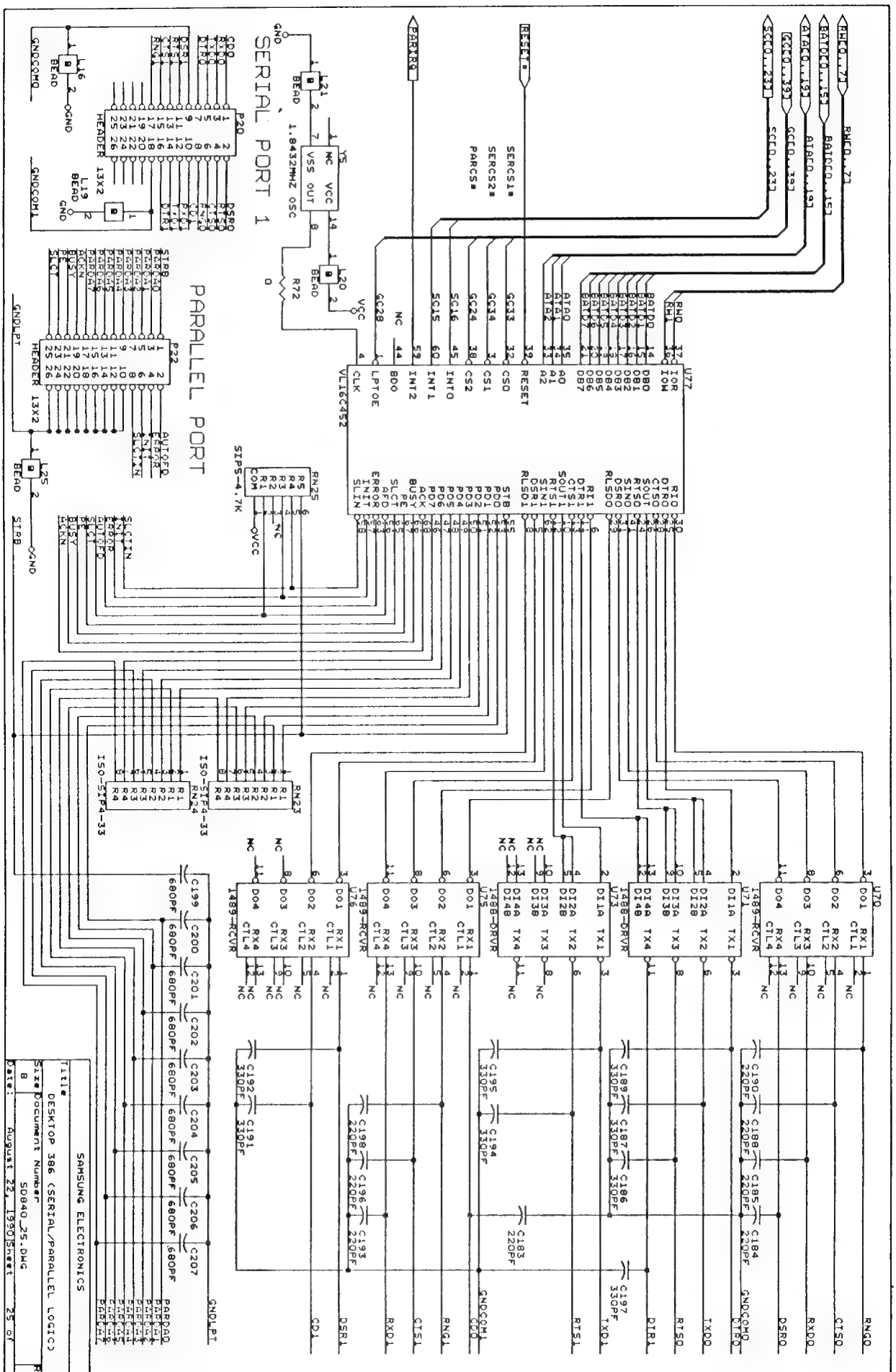
SERIAL PORT 1
PARALLEL PORT
1.8432MHZ OSC
VL16C452
SAMSUNG ELECTRONICS
DESKTOP 386 (SERIAL/PARALLEL LOGIC)
SD840_25.DWG
August 22, 1990
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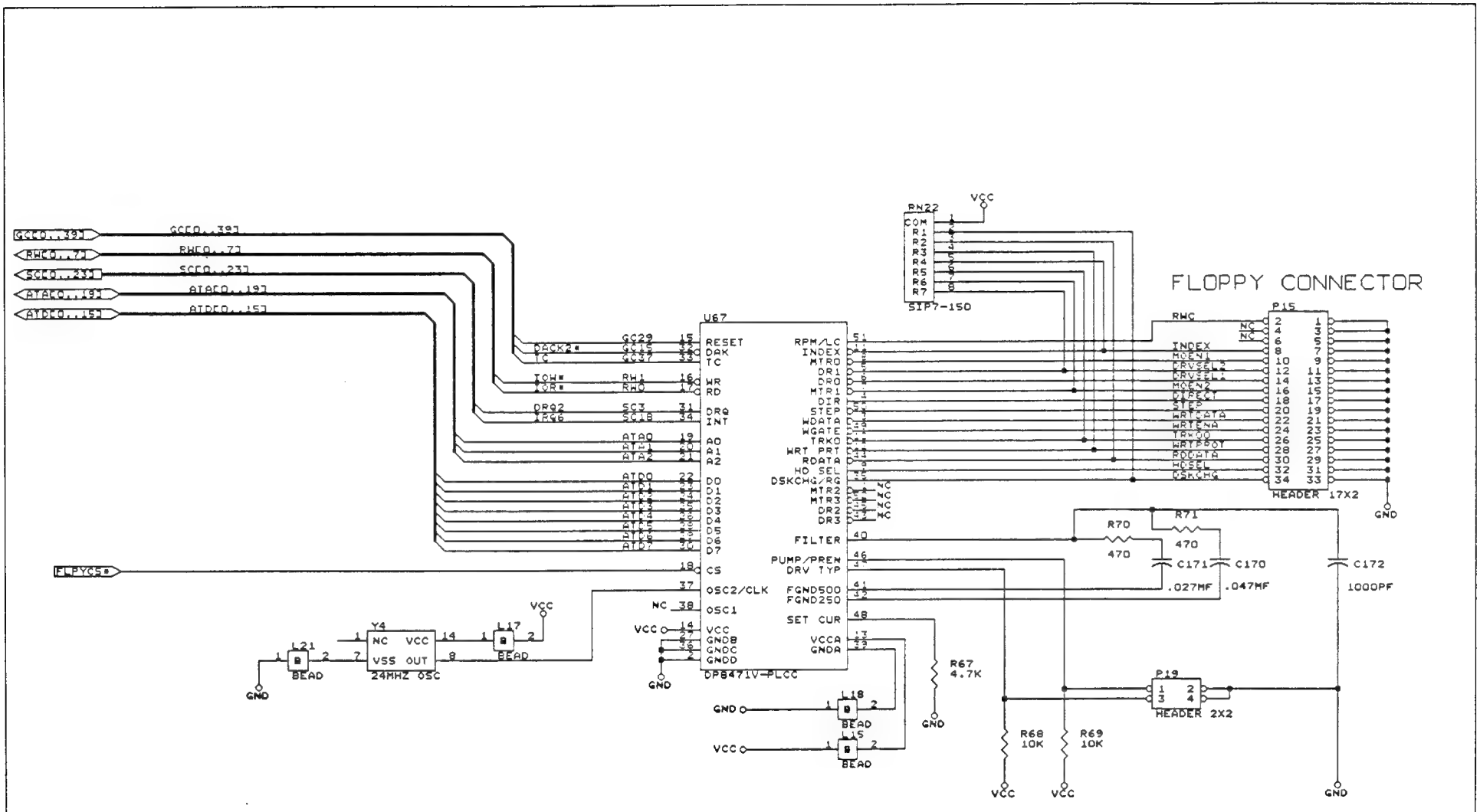
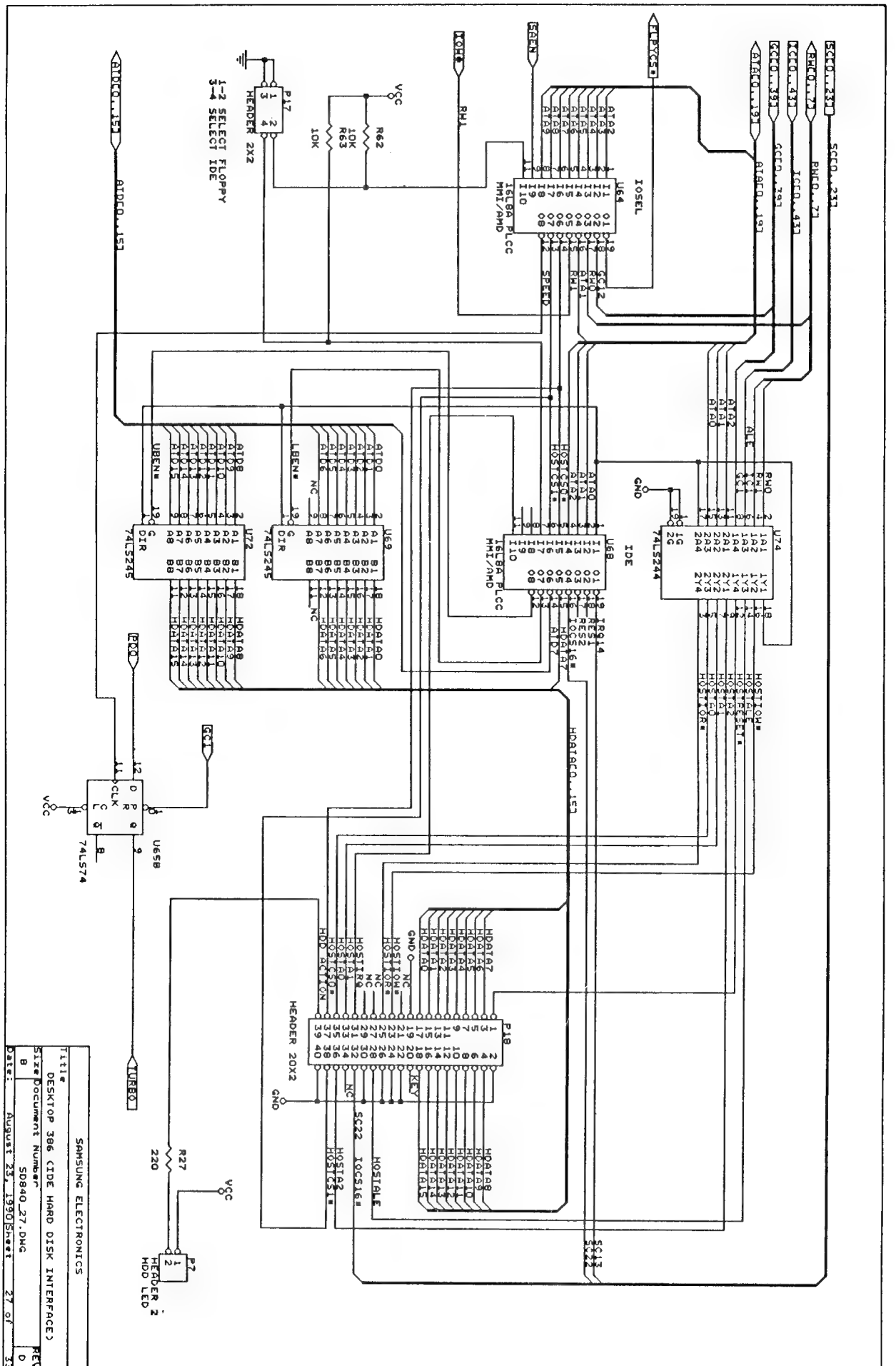
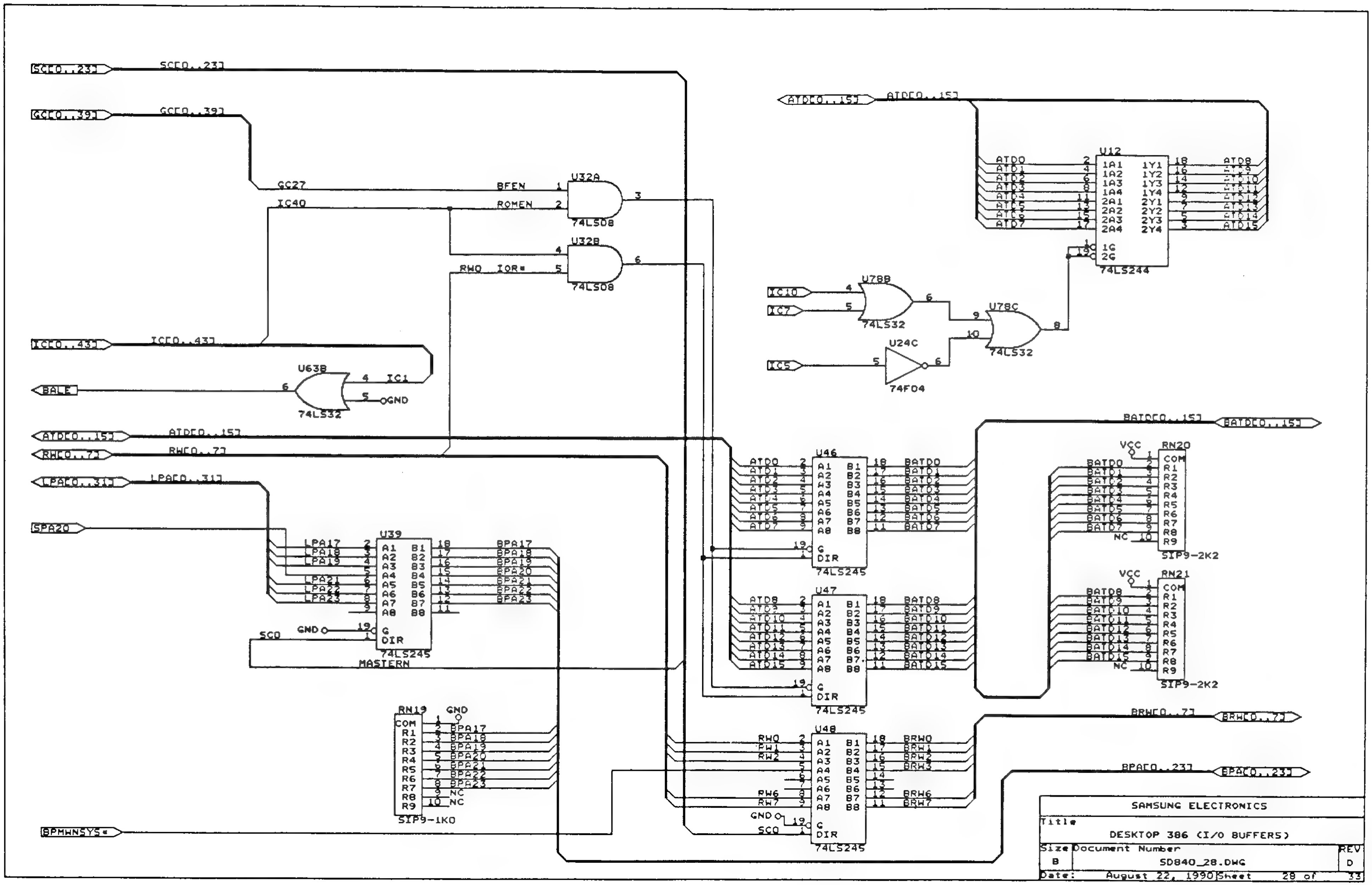
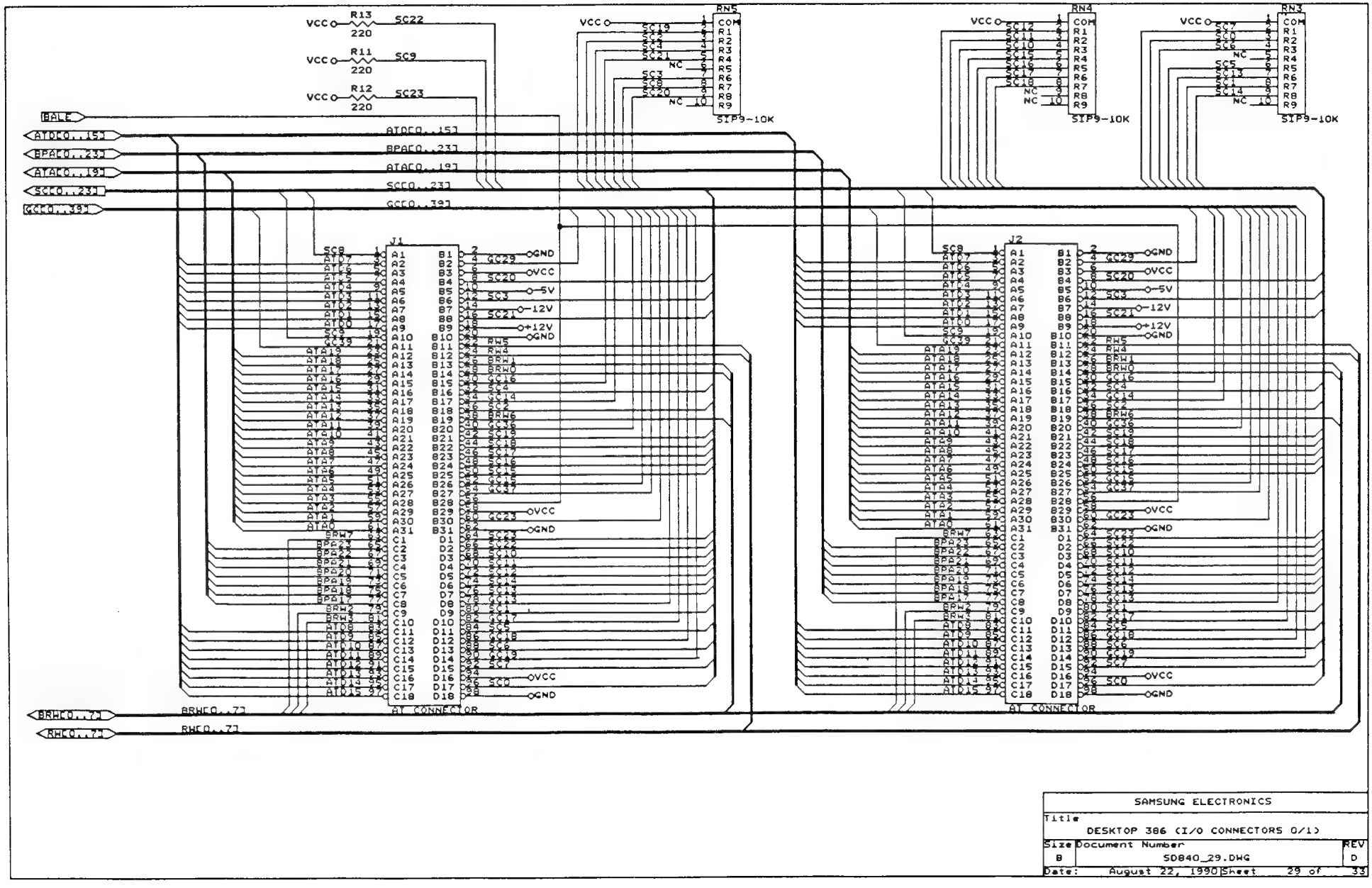


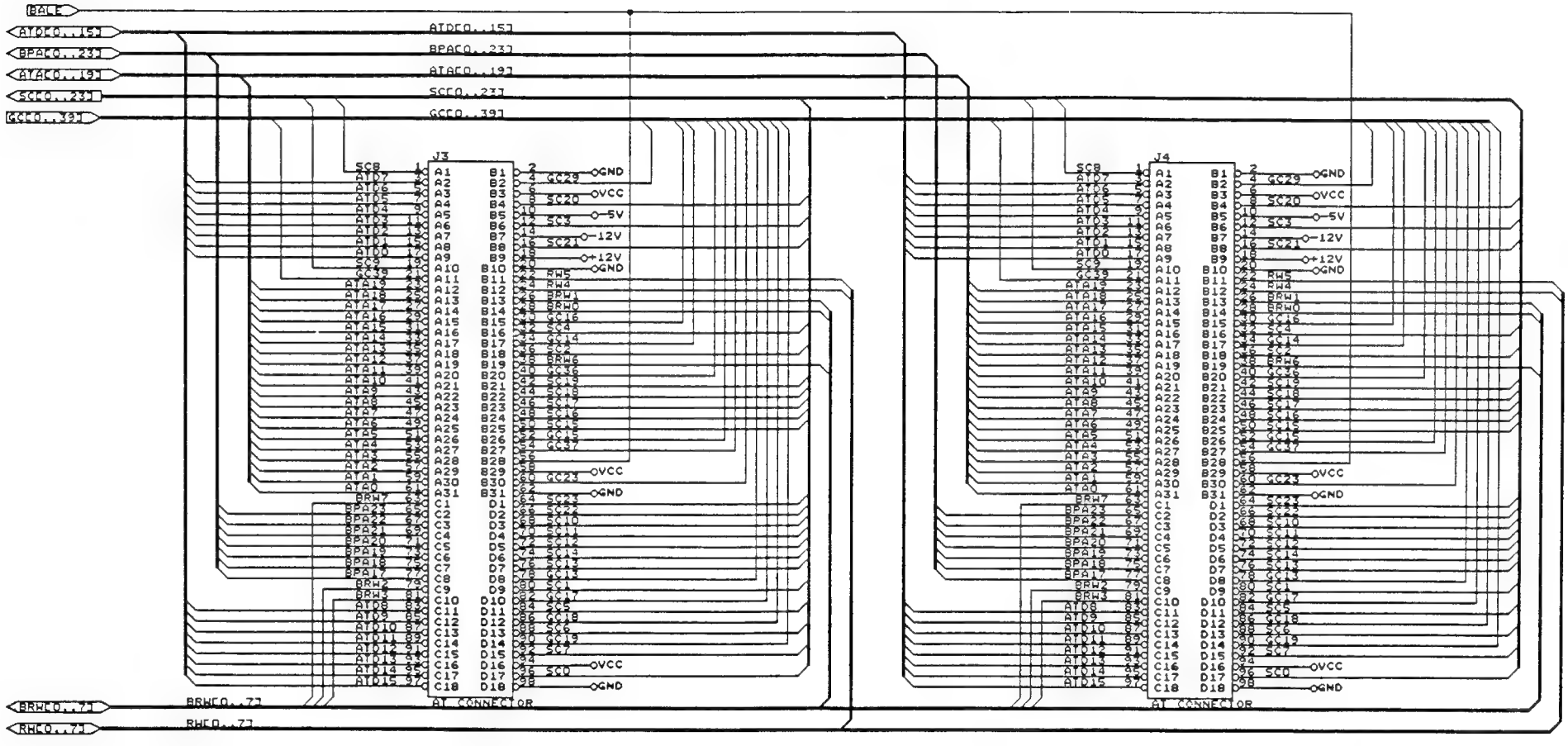
SAMSUNG ELECTRONICS		
Title: DESKTOP 386 (FLOPPY DISK CONTROLLER)		
Size: B	Document Number: SD840_26.DWG	REV: D
Date: August 22, 1990	Sheet 26 of 33	

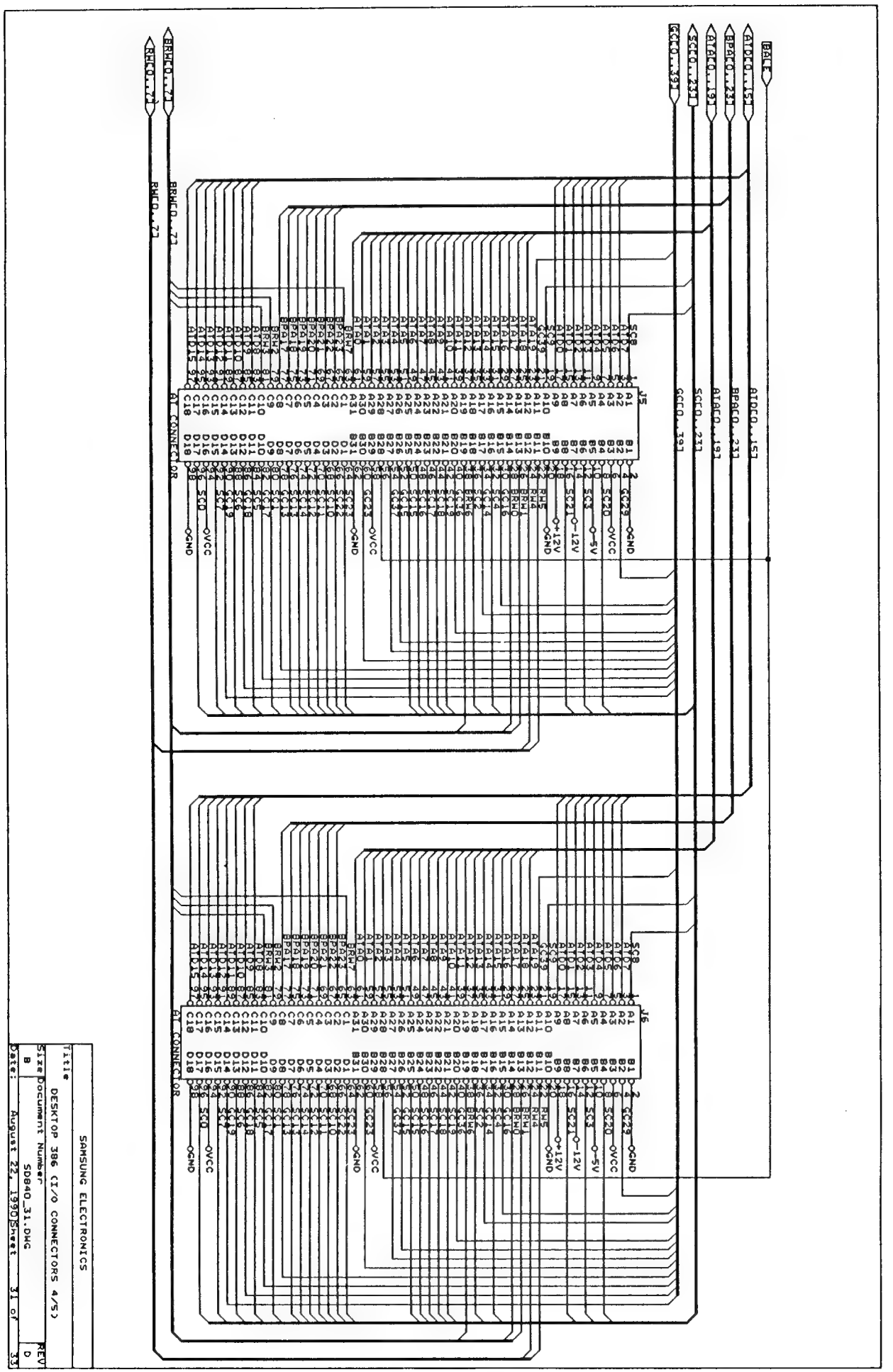

SAMSUNG ELECTRONICS
Title: DESKTOP 386 (IDE HARD DISK INTERFACE)
Size: B
Document Number: 50840_27.DWG
REV: D
Date: August 23, 1990
Sheet 27 of 33
IOSEL
IDE
HEADER 2X2
1-2 SELECT FLOPPY
3-4 SELECT IDE
HEADER 20X2
HEADER 2
HDD LED
74LS245
74LS244
74LS374
I6L8A PLCC
MMI/AMD
R27
220
R62
R63
10K

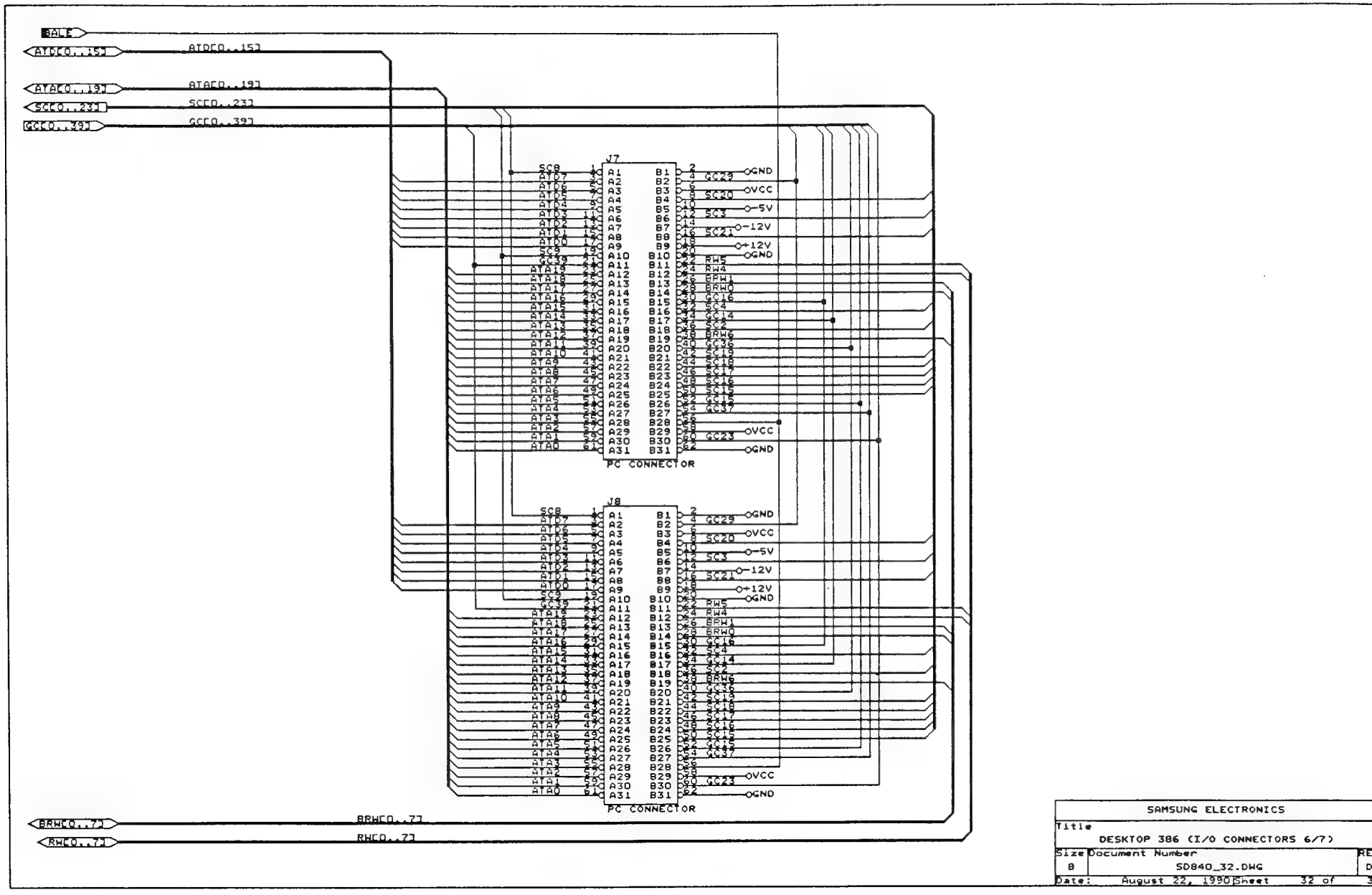

SAMSUNG ELECTRONICS
Title
DESKTOP 386 (I/O BUFFERS)
Size B
Document Number SD840_28.DWG
REV D
Date: August 22, 1990
Sheet 28 of 33
SC[0..23]
GC[0..39]
IC[0..43]
BALE
AT[D[0..15]
RW[0..7]
LPA[0..31]
SPA20
BPMHNSYS*
BATD[0..15]
BRW[0..7]
BPA[0..23]
U32A
U32B
74LS08
U63B
74LS32
U78B
U78C
U24C
74F04
U12
74LS244
U39
U46
U47
U48
74LS245
RN19
SIP9-1K0
RN20
RN21
SIP9-2K2
MASTERN
BFEN
ROMEN
RWO IOR*
GC27
IC40
VCC
GND



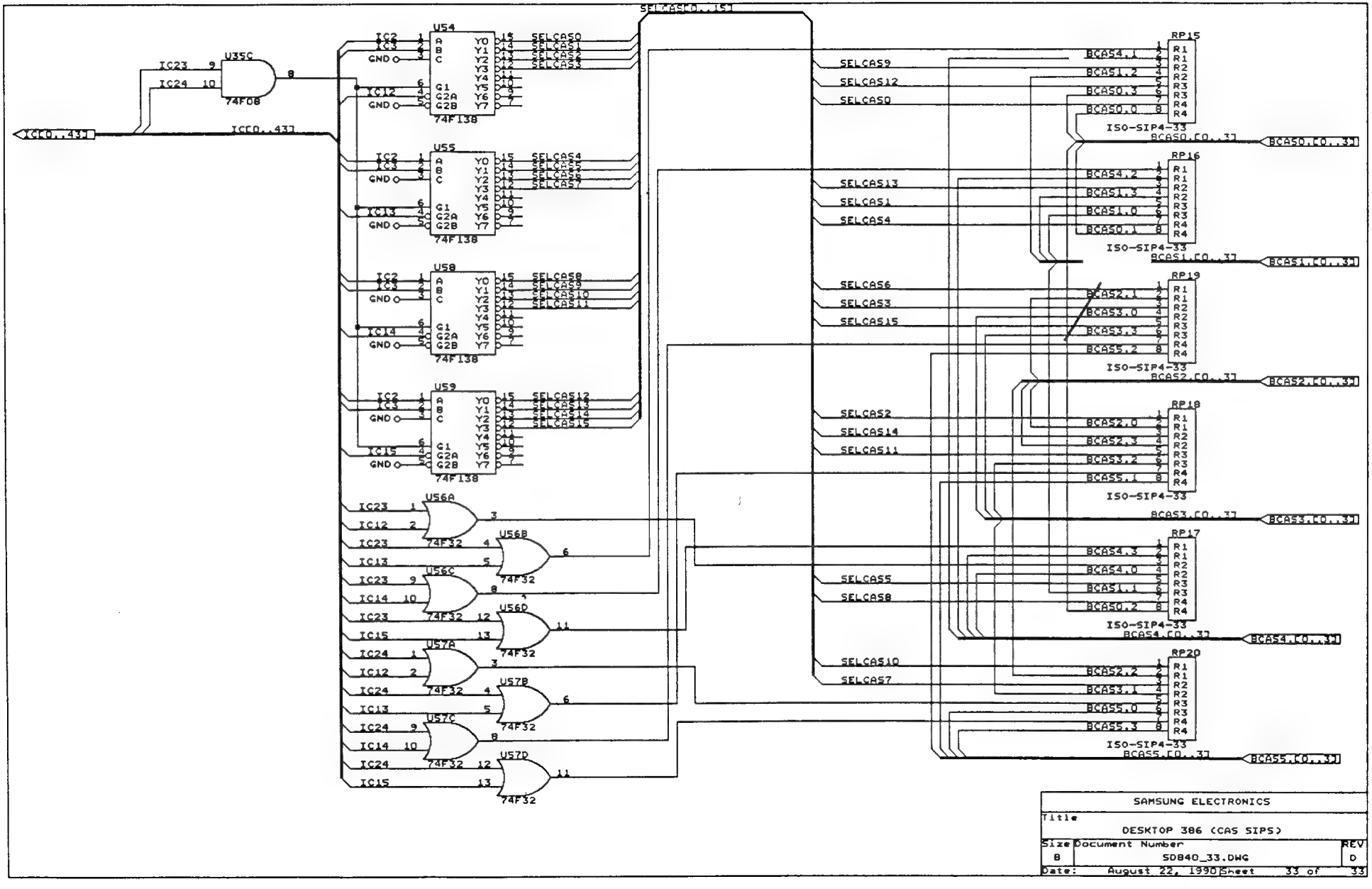
SAMSUNG ELECTRONICS		
Title: DESKTOP 386 (I/O CONNECTORS 0/1)		
Size: B	Document Number: SD840_29.DWG	REV: D
Date: August 22, 1990	Sheet 29 of 33	


BALE
AYDEO..15J
BPAEO..23J
AYAEO..19J
SCEO..23J
GCEO..39J
AIDEO..15J
BPAEO..23J
AIAEO..19J
SCEO..23J
GCEO..39J
J3
J4
AT CONNECTOR
AT CONNECTOR
BRWEO..7J
RWEO..7J
SAMSUNG ELECTRONICS
Title
DESKTOP 386 (I/O CONNECTORS 2/3)
Size
B
Document Number
SD840_30.DWG
REV
D
Date: August 22, 1990 Sheet 30 of 33


SAMSUNG ELECTRONICS
DESKTOP 386 (I/O CONNECTORS 4/5)
SD840_31.DWG
August 22, 1990
J5
J6
EL CONNECTOR



SAMSUNG ELECTRONICS		
Title: DESKTOP 386 (I/O CONNECTORS 6/7)		
Size: B	Document Number: SD840_32.DWG	REV: D
Date: August 22, 1990	Sheet 32 of 33	


SELCAS[0..15]
U35C
74F08
IC23
IC24
IC[0..43]
U54
U55
U58
U59
74F138
SELCAS0
SELCAS1
SELCAS2
SELCAS3
SELCAS4
SELCAS5
SELCAS6
SELCAS7
SELCAS8
SELCAS9
SELCAS10
SELCAS11
SELCAS12
SELCAS13
SELCAS14
SELCAS15
U56A
U56B
U56C
U56D
U57A
U57B
U57C
U57D
74F32
RP15
RP16
RP19
RP18
RP17
RP20
ISO-SIP4-33
BCAS0.[0..3]
BCAS1.[0..3]
BCAS2.[0..3]
BCAS3.[0..3]
BCAS4.[0..3]
BCAS5.[0..3]
SAMSUNG ELECTRONICS
Title
DESKTOP 386 (CAS SIPS)
Size B
Document Number SDB40_33.DWG
REV D
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D

PART LIST

PART LIST

Location No.	Part No.	Description; Specification	Q'ty
	99112 840 000	ASSY MOTHER B/D; 33MHz, SD840 STANDARD	1
R33	91012 165 030	R CARBON (SMD); MCR18J100TA (ROHM)	1
R30	91012 165 031	R CARBON (SMD); MCR18J151TA (ROHM)	1
R46	91012 165 042	R CARBON (SMD); MCR18J680TA (ROHM)	1
R3, 4	91012 165 221	R CARBON (SMD); MCR18J221TA (ROHM)	3
R11-13	91012 165 221	R CARBON (SMD); MCR18J221TA (ROHM)	2
R27, 39	91012 165 221	R CARBON (SMD); MCR18J221TA (ROHM)	2
R35, 56	91012 165 221	R CARBON (SMD); MCR18J221TA (ROHM)	2
R50, 51	91012 165 221	R CARBON (SMD); MCR18J221TA (ROHM)	2
R5	91012 167 203	R CARBON (SMD); MCR18J203TA (ROHM)	1
R17-22	91018 167 000	R CARBON SMD; MCR18J000TA (ROHM)	6
R25, 12	91018 167 000	R CARBON SMD; MCR18J000TA (ROHM)	2
R26, 49	91018 167 102	R CARBON (SMD); MCR18J102TA (ROHM)·RC3216J102CS (SEM)	2
R35, 36	91018 167 102	R CARBON (SMD); MCR18J102TA (ROHM)·RC3216J102CS (SEM)	2
R42-44	91018 167 102	R CARBON (SMD); MCR18J102TA (ROHM)·RC3216J102CS (SEM)	3
R58	91018 167 102	R CARBON (SMD); MCR18J102TA (ROHM)·RC3216J102CS (SFM)	1
R8-10	91018-167-103	R CARBON (SMD); MCR18J103TA (ROHM)·RC3216J103CS (SEM)	3
R14, 54	91018 167 103	R CARBON (SMD); MCR18J103TA (ROHM)·RC3216J103CS (SFM)	2
R31, 32	91018 167 103	R CARBON (SMD); MCR18J103TA (ROHM)·RC3216J103CS (SEM)	2
R40, 41	91018 167 103	R CARBON (SMD); MCR18J103TA (ROHM)·RC3216J103CS (SEM)	2
R47, 48	91018 167 103	R CARBON (SMD); MCR18J103TA (ROHM)·RC3216J103CS (SEM)	2
R57	91018 167 103	R CARBON (SMD); MCR18J103TA (ROHM)·RC3216J103CS (SEM)	1
R59-65	91018 167 103	R CARBON (SMD); MCR18J103TA (ROHM)·RC3216J103CS (SEM)	7
R68, 69	91018 167 103	R CARBON (SMD); MCR18J103TA (ROHM)·RC3216J103CS (SEM)	2
R45	91018 167 330	R CARBON SMD; MCR18J330TA (ROHM)	1
R70, 71	91018 167 471	R CARBON SMD; MCR18J471TA (ROHM)	2
R29	91018 167 472	R CARBON (SMD); MCR18J472TA (ROHM)·RC3216J472CS (SEM)	1
R67	91018 167 472	R CARBON (SMD); MCR18J472TA (ROHM)·C3216J472CS (SEM)	1
R34	91018 167 473	R CARBON (SMD); MCR18J473TA (ROHM)·RC3216J473CS (SEM)	1
R28	91018 277 330	R CARBON; RD 1/4T 33J	1
RN1, 2	91060 106 060	R NETWORK; M06 1 103J (BECKMAN)	2
RN6, 10	91060 106 060	R NETWORK; M06 1 103J (BECKMAN)	2
RN16	91060 108 040	R NETWORK; MO8 1 R1K J (BECKMAN)	1
RN19	91061 102 101	R NETWORK; M10 1 102J (BECKMAN)	1
RN3-5	91061 103 100	R NETWORK; M10 1 103J (BECK MAN)	3
RN22	91061 151 182	R NETWORK; M08 1 151J (BACKMAN)	1
RN7-9	91061 222 100	R NETWORK; M10 1 222J (BECKMAN)	3
RN11-15	91061 222 100	R NETWORK; M10 1 222J (BECKMAN)	5
RN17, 18	91061 222 100	R NETWORK; M10 1 222J (BECKMAN	2
RN20, 21	91061 222 100	R NETWORK; M10 1 222J (BECKMAN)	2
RN23, 24	91061 330 180	R NETWORK SIP; M8 3 330J, 8P (BECKMAN)	2
RN1, 27	91061 330 180	R NETWORK SIP; M8 3 330J, 8P (BECKMAN)	27
RN25	91061 472 160	R NETWORK; M6 1 472J (BECKMAN)	1
C163, 164	91300 314 700	C CERAMIC SMD; 12065A4/0JA1050R (AVX)	2
C166, 167	91300 314 700	C CERAMIC SMD; 12065A4/0JA1050R (AVX)	2
C172	91301 102 356	C CERAMIC, (SMD); 12065C102KAT050R, (AVX)	1

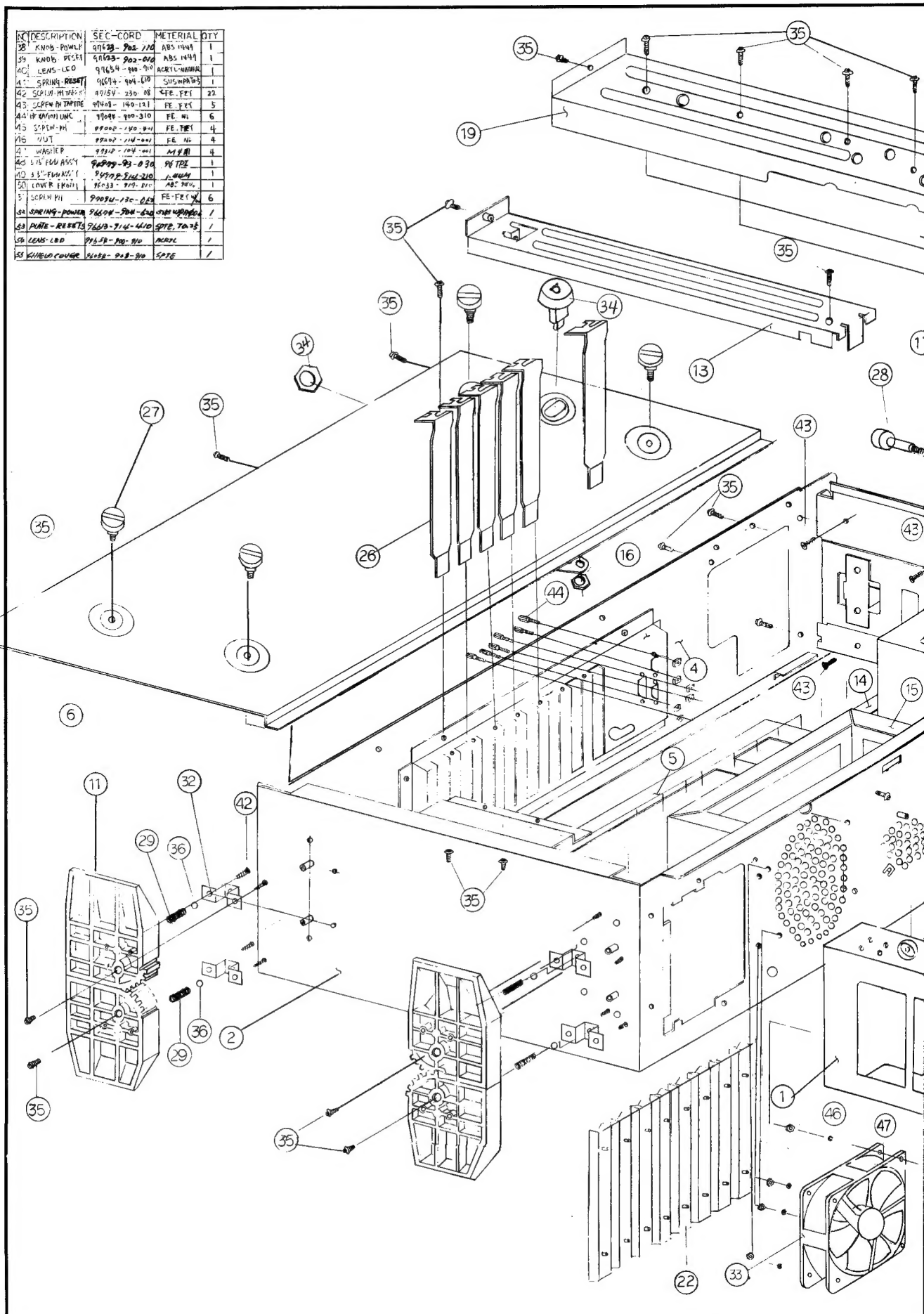
Location No.	Part No.	Description; Specification	Q'ty
C2-5	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	4
C7, 8	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	2
C10-15	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	6
C17-25	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	9
C27-35	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	9
C37-68	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	32
C70-74	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	5
C76-79	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	4
C81, 82	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	2
C84-92	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	9
C94-98	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	5
*C100 9	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	10
*C110 8	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	9
*C123 9	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	7
*C130 4	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	5
*C136 9	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	4
*C140 9	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	10
*C150 9	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	10
*C170 2	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	3
C165	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	1
*C168 9	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	2
*C173 9	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	7
*C180 2	91301 104 756	C MONO CERAMIC SMD; 12065C104KAT060R (AVX)	3
C171	91301 273 156	C CERAMIC SMD; 12065E2/3ZAT050R (AVX)	1
*C186 7	91301 331 650	C CERAMIC (SMD); 12065A331JAT0050R (AVX)	2
C189	91301 331 650	C CERAMIC (SMD); 12065A331JAT0050R (AVX)	1
*C191 2	91301 331 650	C CERAMIC (SMD); 12065A331JAT0050R (AVX)	2
*C194 5	91301 331 650	C CERAMIC (SMD); 12065A331JAT0050R (AVX)	2
C197	91301 331 650	C CERAMIC (SMD); 12065A331JAT0050R (AVX)	1
*C199 7	91301 681 756	C CERAMIC (SMD); 12065A681JAT0050R (AVX)	9
*C183 5	91457 122 200	C MONO CERAMIC SMD; 12061A221JAT060R (AVX)	3
C188	91457 122 200	C MONO CERAMIC SMD; 12061A221JAT060R (AVX)	1
C190	91457 122 200	C MONO CERAMIC SMD; 12061A221JAT060R (AVX)	1
*C193, 6	91457 122 200	C MONO CERAMIC SMD; 12061A221JAT060R (AVX)	2
C198	91457 122 200	C MONO CERAMIC SMD; 12061A221JAT060R (AVX)	1
C170	91457 122 530	C MONO CERAMIC SMD; 12065C473KAT060R (AVX)	1
C1, 6	91609 010 230	C ELECTROLYTIC; SE04W 25V 10MF (SAMHWA)	2
C9, 16	91609 010 230	C ELECTROLYTIC; SE04W 25V 10MF (SAMHWA)	2
*C120 2	91609 010 230	C ELECTROLYTIC; SE04W 25V 10MF (SAMHWA)	2
*C26, 36	91609 010 230	C ELECTROLYTIC; SE04W 25V 10MF (SAMHWA)	2
C69	91609 010 230	C ELECTROLYTIC; SE04W 25V 10MF (SAMHWA)	1
C119	91609 010 230	C ELECTROLYTIC; SE04W 25V 10MF (SAMHWA)	1
C208	91609 010 230	C ELECTROLYTIC; SE04W 25V 10MF (SAMHWA)	1
*C75, 80	91609 010 230	C ELECTROLYTIC; SE04W 25V 10MF (SAMHWA)	2
C83, 93	91609 010 230	C ELECTROLYTIC; SE04w 25V 10MF (SAMHWA)	2
C99	91609 010 230	C ELECTROLYTIC; SE04W 25V 10MF (SAMHWA)	1
C135	91609 010 230	C ELECTROLYTIC; SE04W 25V 10MF (SAMHWA)	1
U41, 49	92109 337 200	IC EPROM; 2/C256 20 (SIG)	2

Location No.	Part No.	Description; Specification	Q'ty
U6 7	92109 350 082	IC SRAM (PLCC); V63C328J03 (VITELIC)	2
U18 19	92109 350 082	IC SRAM (PLCC); V63C328J03 (VITELIC)	2
U36	92109 400 020	IC CPU MFMORY CONTROLLER; GC132C (LSI LOGIC)	1
U33	92109 400 030	IC GLUE (PLCC); L4A8024 (LSI LOGIC)	1
U5	92109 400 040	IC CACHE CONTROLLER; A38202 33 QFP (AUSTEK)	1
U42	92109 400 050	IC RTC; DS1287 (DALLAS)	1
U37	92109 400 060	IC BUS BRIDGE INTERFACE; GC133B (LSI LOGIC)	1
U30	92109 400 070	IC PERIPHERAL CONTROLLER; GC131B (LSI LOGIC)	1
U50	92109 401 070	IC CPU; D8742 (IN/SSI)	1
U8	92109 401 380	IC CPU; 180386DX 33, PGA (INTEL)	1
U67	92109 406 130	IC FDC (PLCC); DP8473 PLCC (NS)	1
U67	92109 406 140	IC FDC (PLCC); DP8471 PLCC (NS)	0
U16	92109 502 404	IC TTL (SMD); 74AC1240 (NS)	1
U66	92109 510 061	IC TTL (SMD); SN7406 (TI)	1
U32, 40	92109 520 81	IC TTL (SMD); SN74LS08 (TI)	2
U34	92109 520 141	IC TTL (SMD); SN74LS14D (TI)	1
U63, 78	92109 520 321	IC TTL (SMD); SN/4LS32 (TI)	2
U65	92109 520 741	IC TTL (SMD); SN/4LS74AD (TI)	1
U74	92109 522 441	IC TTL (SMD); SN74LS244D (TI)	1
U39, 48	92109 522 451	IC TTL (SMD); SN74LS245D (TI)	2
U46, 47	92109 522 451	IC TTL (SMD); SN74LS245D (TI)	2
U69, 72	92109 522 451	IC TTL (SMD); SN74LS245D (TI)	2
U24	92109 540 044	IC TTL (SMD); 74F04 (NS)	1
U35	92109 540 084	IC TTL (SMD); 74F08 (NS)	1
U1, 3	92109 540 324	IC TTL (SMD); 74F 32SC (NS)	2
U56, 57	92109 540 324	IC TTL (SMD); 74F 32SC (NS)	2
U79	92109 540 324	IC TTL (SMD); 74F 32SC (NS)	1
U13	92109 540 745	IC TTL (SMD); N74F74D (SIG)	1
U54, 55	92109 541 385	IC TTL (SMD); N74F138D (SIG)	2
U58, 59	92109 541 385	IC TTL (SMD); N74F138D (SIG)	2
U31	92109 541 754	IC TTL (SMD); 74F175SC (NS)	1
U38	92109 542 444	IC TTL (SMD); 74F244SC (NS)	1
U43-45	92109 542 444	IC TTL (SMD); 74F244SC (NS)	3
U51-53	92109 542 444	IC TTL (SMD); 74F244SC (NS)	3
U60-62	92109 542 444	IC TTL (SMD); 74F244SC (NS)	3
L20-23	92109 553 741	IC TTL (SMD); SN74AS374 (TI)	4
U26-29	92109 556 464	IC TTL (SMD); DM74AS646 (NS)	4
U77	92109 911 680	IC CUSTOM 170 (PLCC); 82C452A (SIS)	1
U64, 68	92109 912 141	IC PAL (PLCC); PAL16l8ACNL (MMI)	2
U9	92109 916 010	IC PAL (PLCC); PAL16L8 ECN (MMI)	1
U10, 11	92109 916 020	IC PAL; 20LB ECN (MMI)	2
U71, 73	92109 921 190	IC DRIVER (SMD); SN75188D (TI)	2
U70	92109 923 010	IC RECEIVER (SMD); SN75189D (TI)	1
U75, 76	92109 923 010	IC RECEIVER (SMD); SN75189D (TI)	2
Q1	92149 403 630	TRANSISTOR; PN2222 (SSI)	1
D1	92169 210 071	DIODE (SMD); LL4148F (ITF)	1
	93004 480 001	PWB MAIN; 350×305, 6LAYER (SD840)	1
JUMP	93340 502 230	CONNECTOR B JUMP; 90059 0014, 2P (MOL KOR)	12

Location No.	Part No.	Description; Specification	Q'ty
J7, 8	93340 762 030	CONNECTOR CARD EDGE; SQ 2500 62 (LEADER)	2
J1, 6	93340 798 010	CONNECTOR CARD EDGE; 645169 2 (AMP) (DUAL 18 & 31)	
J9	93340 905 040	CONNECTOR DIN; 57PC5PS (SWITCHCRAFT)	1
P2, 3, 7	93341 002 001	CONNECTOR HEADER; SPS04 S02G (WOO YOUNG)	3
P10-13	93341 002 001	CONNECTOR HEADER; SPS04 S02G (WOO YOUNG)	4
	93341 002 100	CONNECTOR HEADER; SPS04 S02G (WOO YOUNG)	3
	93341 002 100	CONNECTOR HEADER; SPS04 S02G (WOO YOUNG)	4
P1	93341 003 080	CONNECTOR HEADER; SPS04 03 (SINGLE 3PIN)	1
P8	93341 004 130	CONNECTOR HEADER; SPS04 S04G (WOO YOUNG)	1
P20, 22	93341 026 040	CONNECTOR HEADER; SPS04 D26G (WOO YOUNG)	2
P15	93341 034 030	CONNECTOR HEADER; SPS04 D34A4 (WOO YOUNG)	1
P18	93341 040 020	CONNECTOR HEADER; SPS04 D40G (WOO YOUNG)	1
P19	93345 021 041	CONNECTOR HEADER; SPS04 D04A (WOO YOUNG)	1
P16, 17	93345 021 041	CONNECTOR HEADER; SPS04 D04A (WOO YOUNG)	2
P9	93345 021 050	CONNECTOR PIN HEADER; SPS04 S5A4 (WOO YOUNG)	1
SM1-24	93345 039 600	CONNECTOR SIMM SOCKET; 821885 2 (AMP)	12
J10	93345 051 000	JACK DIN; LN 0508A 6A (LIB SHFNG)	1
P14	93345 077 060	CONN HEADER (PWR); GTC6R 1 (BURNDY)	2
U42	93354 124 010	SOCKET IC; WSDIF 24P (WOO YOUNG)	1
U10, 11	93354 124 280	SOCKET IC; WSDIF 24N (WOO YOUNG)	2
U41, 49	93354 128 010	SOCKET IC; WSDIF 28P (WOO YOUNG)	2
U8	93354 132 040	SOCKET EMC; 550 114 132 (TEKCON)	1
USO	93354 140 010	SOCKET IC; WSDIF 40P (WOO YOUNG)	1
U2, 4	93354 152 010	SOCKET IC; 821551 1, PLCC (AMP)	2
U14, 15	93354 152 010	SOCKET IC; 821551 1, PLCC (AMP)	2
U33, 77	93354 168 060	SOCKET IC 68P; 821689 1 (AMP) PLCC	2
SKT1	93354 905 520	SOCKET EMC; 550 113 121 (TEKCON)	1
L7-9	94049 903 160	FERRITE BEAD; 2943666671	3
L10, 24	94049 903 160	FERRITE BEAD; 2943666671	2
L1-6	94049 903 941	FERRITE BEAD (SMD); 2743019447 (F/R)	6
L11-23	94049 903 941	FERRITE BEAD (SMD); 2743019447 (F/R)	13
Y3	94539 066 670	OSC NETWORK; NSA0184, 66.67MHz (NDK)	1
Y4	94539 911 810	OSC CLOCK; SCO 010K 24.0000 MHz (SUNNY)	1
Y1	94539 915 380	OSC CLOCK; SCO 020K 32.0000 MHz (SUNNY)	1
Y5	94539 915 400	OSC CLOCK; SCO 010W 1.8432 MHz (SUNNY)	1
Y2	94539 915 910	OSC CLOCK; SCO 010T 28.63636 MHz (SUNNY)	1
F1	94709 902 710	PICO FUSE: 251004 (LITTEL)	1
	96674 905 710	SPRING CONTACT KBD; PBSP T0.6	1
	99112 840 021	ASSY DRAM PART; 4MB (1MB*4), SD840	1
	92109 369 011	IC DRAM MODULE; KMM591000A 08 (SEC)	4

Location No.	Part No.	Description; Specification	Q'ty
	97094 130 062	SCREW PH; M3S6 FE FZW W/WASHER	3
COVER	97094 970 610	BOLT SPECIAL; SUM24L NI PLATED	4
BEZEL	97154 230 081	SCREW TAP PH; 2S 3XB FE FZY W/WASHER	8
	97624 904 069	KNOB POWER; ABS 94V0 AF 303 1447 (SISA)	1
	90742 185 069	RESIN ABS; AF 303 1447 94VO BEIGE	0.00305 (KG)
	97624 904 510	KNOB RESET; ABS 94VO AF 303 1447 (SISA)	1
	90742 185 069	RESIN ABS; AF 303 1447 94VO BEIGE	0.00265 (KG)
	97654 900 910	LENS LED; ACRIYL SEMI CLEAR WHITE	1
	99111 840 004	ASSY BOTOM; SD840 (STANDARD)	1
STAND	94544 901 910	PLATE STAND, R; SUS304 10-3	2
STAND	94544 901 920	PLATE STAND, L; SUS304 10-3	2
STAND	95104 901 010	SHAFT STAND; SUM24L FZW	2
STAND	95104 901 110	BOLT STAND; SUM24L FZW	2
CHASS	96011 900 310	COVER TOP; ABS 94VO AF 303 1447	1
CHASS	96642 900 010	STAND (R); ABS 94VO AF 303 1447	2
CHASS	96642 900 020	STAND (L); ABS 94VO AF 303 1447	2
STAND	96674 902 010	SPRING POWER; SUS WPA P10.5, ST 35	2
STAND	96674 904 310	SPRING STAND; SUS WPA 10.5	4
MBOARD	97088 130 062	SCREW BH; M3*6 FE FZW	8
	97094 130 062	SCREW PH; M3*6 FE FZW W/WASHER	3
HANDLE	97094 970 520	BOLT HANDLE; SUM24L NI PLATED	2
	97154 230 081	SCREW TAP PH; 2S 3×8 FE FZY W/WASHER	8
CHASS	97408 140 121	SCREW TAPTITE, PH; 1B 4*12 FE FZY	5
TOP	97662 900 010	HANDLE; ADC 12 COATING	1
STAND	98404 970 210	BALL STAND; STEEL 16.4	2
	99113 610 015	ASSY VIDEO BOARD; GTI VGA	1
	90469 100 006	SOLDER FLUXCORE WIRE; P1 1.0 SN63 PB37	0.01000 (KG)
	90469 100 007	FLUX; KESTER 2331	0.50000 (LT)
	90469 100 008	SOLDER WIRE; SN63 PB37 3.0W WATER (DONG YANG)	0.50000 (KG)
	90469 120 610	SOLDER SMD; FC 70 (FLUORINERT 3M)	0.00230 (KG)
	90519 900 310	WIRE WRAP; BE03A040 (26AWG) BLU (JUNKOSHA)	0.30000 (MT)
	90849 012 100	CLEAR PCB; FLON 113 (FREON 113, TF, TES)	0.02000 (KG)
R2	91018 277 101	R CARBON; RD 1/4T 100 J	1
R7	91018 277 102	R CARBON; RD 1/4T 1K J	1
R1	91018 277 103	R CARBON; RD 1/4T 10K J	1
R6	81018 277 361	R CARBON; RD 1/4T 360 J	1
	91018 377 333	R CARBON; RD 1/2T 33K J	1
U04, 08	91060 108 170	R NET; L08 1 103 (10K 8P) (BECK MAN)	2
U12	91061 103 100	R NETWORK; M10 1 103J (BECK MAN)	1
RN5	91061 151 180	R NETWORK; M8 3 151J (BECK MAN)	1
RN3, 4	91061 333 100	R NETWORK; M10 3 333J (BECK MAN)	2
U11, 14	91061 333 180	R NETWORK; M8 1 333J (BECK MAN)	2

E. EXPLODED VIEW



NO	DESCRIPTION	SEC-CORD	METERIAL	QTY
38	KNOB-POWER	97629-902-110	ABS 1449	1
39	KNOB-RESET	97633-902-010	ABS 1449	1
40	LENS-LED	97654-900-910	ACRYL-NATURAL	1
41	SPRING-RESET	96694-904-610	SUS-WPB75	1
42	SCREW-M TAPPING	97154-230-08	SPCC, FEY	22
43	SCREW-M TAPPING	97408-140-121	FE, FEY	5
44	HEXAGON UNC	97098-900-310	FE, Ni	6
45	SCREW-PH	97008-140-811	FE, FEY	4
46	NUT	97207-114-001	FE, Ni	4
47	WASHER	97318-104-001	M1 #1	4
48	5.25" FDD ASSY	96899-93-030	96 TPE	1
49	3.5"-FDD ASSY	96999-S14-210	1.4MB	1
50	COVER FRONT	96933-919-811	ABS 94V0	1
51	SCREW PH	97034-130-062	FE-FEY	6
52	SPRING-POWER	96604-904-620	SWP-B	1
53	PLATE-RESET	96613-914-410	SPTE, T0.25	1
54	LENS-LED	96658-900-910	ACRYL	1
55	SHIELD COVER	96088-908-910	SPTE	1

품번	명 칭	도 번	재 질	수량	소재치수	절적치수	비 고

NO	DESCRIPTION	SEC - CORD	METERIAL	QTY
1	BRKT-HDD	96611-903-010	EGI T1.2	1
2	CHASSIS-MAIN	96121-905-710	EGI T1.2	1
3	BRKT-FDD	96121-905-610	EGI T1.0	1
4	CHASSIS-BACK	96121-905-510	EGI T1.2	1
5	BRKT-PCB BASE	96121-905-410	EGI T1.0	1
6	CHASSIS-COVER	96121-905-210	EGI T1.2	1
7	BRKT-HDD BLANK	96612-907-110	EGI T1.0	1
8	BEZEL-FRONT	96001-974-210	ABS 1847	1
9	SMPS-LAF-OUT	94969-905-060		1
10	HANDLE	97662-900-010	EnPC 2	1
11	STAND(R/L)	96682-900-010	ABS 946	4
12	BRKT-HANDLE	96612-908-710	EGI T1.2	1
13	BRKT-ANGLE	96612-908-610	EGI T1.0	1
14	BRKT-HDD BASE	96612-908-510	EGI T1.2	1
15	BRKT-GUIDE SPK	96612-908-420	EGI T1.0	1
16	BRKT-REAR	96612-907-910	EGI T1.2	1
17	COVER-TOP	96011-900-310	ABS 946	1
18	BRKT-SPACER	96612-906-022	EGI T1.0	1
19	BRKT-LINK	96122-901-310	EGI T1.0	1
20	BEZEL-RESET	96082-980-710	ABS 1847	1
21	BRKT-FDD RAIL	96614-916-610	EGI T1.0	3
22	GUIDE-PCB	96463-902-210	POLY CARBONATE	8
23	COLOR-BAR A	96083-920-610	ABS 1847	1
24	COVER-FRONT	96053-919-8	ABS 946 MILK WHITE	1
25	SHIELD-PLATE	98849-902-02	SBHG AT1.0	1
26	BRKT-BLANK	96124-971-920	SPC-1 NI 도금	
27	BOLT-SPECIAL	97094-970-610	SUM 24L NI 흑	4
28	BOLT-HANDLE	97094-970-520	SUM 24L NI 도금	2
29	SPRING-STAND	96694-904-NB	STSCP304 Φ0.5	4
30	BRKT-TENSION	96614-916-110	SUS T0.3	4
31	COLOR-BAR B	96054-920-910	ABS 1847	1
32	PLATE-STAND	97454-901-910	SUS304 T0.4	4
33	FAN	98709-901-510		1
34	KEY-LOCK ASSY	96346E-700-340	ZN/NI PLATED	1
35	SCREW PM	99094-130-062	FE FBW	58
36	BALL-STAND	98446-970-2	STEEL	4
37	SPEAKER	96208-302-810		1

년 월 일	서 명	변 경 사 항					변 경 사 유
단위	사도	제도	설계	검도	심사	승인	EXPLODED-VIEW
척도 N.S	박근호		고천형				
공차	97.11.14		97.11.14	97.11.14			

삼성전자주식회사

STOCK NO. | 검 경 도 번 | 도번 번호